UNIVAC® II

ANALYSIS OF INSTRUCTIONS

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UNIVAC II

ANALYSIS OF INSTRUCTIONS

VOLUME III

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LIST OF ILLUSTRATIONS

1. GENERAL .

The "Analysis of Instructions" manual contains three sections relevant to the analysis and understanding of the routines performed by the computer. These sections include 1) a format which relates the discrete operations of each sequence by description, and with the corresponding control Function Table (FT) signal, in such a manner that the time of occurrence of each operation is clearly delineated; 2) a roster of the computer routines by code with the Function Table signals as they appear with regard to time of occurrence in the routine; and 3) a list of the Function Table signals with pertinent information concerning each signal.

The basic period in the performance of an instruction routine is the Program Counter (PC) step. Depending on the complexity of the routine, the number of PC steps varies: only one is required to conclude many instructions, while sixteen are required for the division, D, routine. Each PC step is comprised of two distinct cycles, the Time-out (TO) cycle and the Time-on cycle (exceptions to this occur in the division, multiplication, and shift routines). Time-out is always one minor cycle (91 pulse times) in duration. Time-on, however, exists for as long a period as is necessary to complete the operations required during a particular PC step. Time-out provides time for the FT signals to become fully alerted and to perform some operations that require no FT signals. Time-on determines the life of the FT signals and, therefore, is essentially the time in which the operations to be performed during a PC step are accomplished.

The Function Table signals provide most of the control necessary to accomplish the computer routines. Each FT signal provides a unique function, the proper combination of which enables the computer to execute the various instructions. There are 101 discrete FT signals. For purposes of identification these are numbered, the numbers ranging between 100 and 861. The appropriate FT

signals are alerted by a signal generated from the proper combination of the instruction character code and the PC step during which the routine produced by the FT signal is to occur. A descriptive presentation of the FT signal decoding is made in Figure 1, page 91.

The PC steps and the FT signals provide the basis for the instruction analysis. Subroutines occurring in the proper sequence produce the routines specified by the instructions.

2. GLOSSARY OF ABBREVIATIONS AND SYMBOLS.

AOC	All Ones Checker
BC	Binary Counter
BCI	The binary counter which controls the order, right-hand or left-hand, of reference to a word in register I.
BCM	The binary counter which controls the order, right-hand or left-hand, of reference to a word in main memory.
BCO	The binary counter which controls the order, right-hand or left-hand, of reference to a word in register O.
BIR	Backward Interlock Release signal
BP	Backward Pick-up signal
CC	The Control Counter
Comp	Comparison
CR1	The 91 pulse register of the Control Register
CR2	The 42 pulse register of the Control Register
CT	Conditional Transfer
CU	The Cycling Unit
CY	The Cycle Counter
EP	Ending Pulse
FF	Flip-flop
FIR	Forward Interlock Release signal
FIR-BIR	The Uniservo tape is in the First Block condition.
FT	Function Table
FTIC	The Function Table Intermediate Checker
FTOC	The Function Table Output Checker
HSB	The High-Speed Bus
IER	The multiplIER signal
IER-OR	A signal used by both multiplication and division routines
IO-INT	Input-Output Interlock checker

IOS	Interrupted Operation Switch
IRG	Interlock Release Gate output
IRP	Interlock Release Pulse
LE	Leading Edge
LM	Left-hand section of the main memory
LSB	Least Significant Bit
LSD	Least Significant Digit
M_1	The half-word magnetic switching core register of the rM Bit Plane Control
M_2	The half-word magnetic-switching core register of the rI Bit Plane Control
M_3	The half-word magnetic-switching core register of the rO Bit Plane Control
M_4	The half-word magnetic-switching core register of the Output Distributor
min	Minuend
MQC	The Multiplier-Quotient Counter
MQC-FT	The output matrix of MQC
MSD	Most Significant Digit
MTO	Memory Time Out
N_5	The seven-bit magnetic-switching core register of the Input Distributor
nS	Uniservo selector signal
OE	Odd-Even
OEC	Odd-Even Checker
OR	The divisOR signal
PC	The Program Counter
PPI	Pulses per inch
PS	Pulse Stretcher
rA	The one-word A register

rF	The one-word F register
rI	The 60-word I register
rL	The one-word L register
rM	The 2000 word main memory register
RM	The right-hand section of the main memory
rO	The 60-word O register
RP	The Read Pick-up signal
rW	The ten-word W register
rX	The one-word X register
rZ	The 60-word Z register
S/NS	Signal/No Signal
S1CP	The subtraction signal generated in CP (operate the complementer)
S1X	The subtraction signal generated in MQC (operate the complementer)
S2	Switch inputs to AA
SC	Supervisory Control
SCI-CR	Type into CR from SC
sub	Subtrahend
t	t pulses - any of the timing pulses in the 91 pulse cycle generated by CU
TE	Trailing Edge
TO	Time-Out
TRI	Input section transfer pulses
TRO	Output section transfer pulses
TT	Test Terminal
TZ	Through-zero
WP	The Write Pick-up signal
Z	Decimal zero
( )	The contents of
$\longrightarrow$	Transmit
$\underline{m}$	A word in rM from which a specified field is selected
$\overline{rx}$	Duplicated X register

3. ANALYSIS OF INSTRUCTIONS.

This section provides a detailed analysis of the various computer instructions. The instructions are listed in the binary order of the character code which specifies the routine. This code occupies the first-character position of the six-character instruction word. Where the instruction routine is altered by a symbol in the second character position, the routine is again presented but with the modification that has been made. An "F" in the second instruction character "field selects" the operand as it is transferred from storage and an "H" returns the results of an operation to storage. For the input-output operation, the second instruction character addresses the Uniservo required by the instruction. Other instruction modifications are made by use of the second instruction character. These are described in the instructions concerned. The "m" section of the instruction word designates an address in storage.

The analysis of each instruction begins with a shorthand presentation of the routine to be accomplished by the instruction. Following this, and organized with regard to time of occurrence; i.e., by PC steps, is a description of the functions performed by the various FT signals that are alerted for the routine. In the column to the right of the page is the number of the FT signal described. Appropriate footnotes are supplied where clarification or qualification is necessary.

The CY outputs of β, β COMPUTE, γ, and δ and the RETAIN INSTRUCTION routine are not considered instructions, but they do control FT signals as part of the automatic internal programming of the computer. The routine accomplished during these cycles and the FT signals required to perform these routines are described on page 7.

INSTRUCTION	DESCRIPTION	FT
Beta	(CC) + 1⟶CC; LH (CR)⟶SR Distributor	
	Set up adder for twelve-place addition.	714
	Operate adder OE and sum comparison checkers.	435
	Connect CR1 to SR Distributor Line.	204
	Connect CC to adder min input, Cycling Unit (000000 000001) to adder sub input. Clear CC and read the sum from the unbarred adder to CC.	
	(Transfer to CC ends t12 of TO).	212
	Supply reset pulse to Overflow FF's	737
Beta Computer	(m)⟶CR	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM	827
	Operate HSB - OEC.	429
	Operate HSB - AOC.	428
	Set rM Read FF, set M1 cores.	820
	Strobe, rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to CR, and clear CR.	201
	Set MTO.	825
	Supply EP.	206
	(rM address sets up at t7 of Beta TO, unless overflow occurs, which delays Set-up until t35, thereby setting SR to Z's.)	
Gamma	RH(CR)⟶SR Distributor; Execute LH instruction.	
	Connect CR1 to CR2.	203
	(LH Instruction sets up at t7 of Gamma TO)	203K
Delta	RH(CC)⟶SR Distributor; Execute RH Instruction.	
	Connect CC to SR via CR2#.	850
	#RH Instruction is set up at t7 of Delta TO.	203K
RETAIN INSTRUCTION	Repeat routine performed during a selected CY cycle.	
	β cycle: Inhibit FT 201, 204,212, 435; Alert FT 850	
	γ cycle: Inhibit FT 203; Alert FT 204, 203K and specified instruction FT signals	
	δ cycle: Inhibit FT 850; Alert FT 203, 203K and specified instruction FT signals	

INSTRUCTION	DESCRIPTION	FT
A 0 m	(m) → rX; (rX) + (rA) → rA.	
1.	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB - OEC.	429
	Operate HSB - AOC.	428
	Set rM Read FF, set M1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rX.	126
	Operate rX clear gate.	120
	Set MTO.	825
	Step PC, set TO.	214
TO	Compare (rA) and (rX).	NONE
2.	Operate adder for eleven-place addition.*	160
	Operate adder OE and sum comparison checkers.	435
	Connect rX to HSB.	125
	Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. (Transfer to rA ends at t12 of TO)	109
	Supply EP.	206
	*If decimal carry occurs from eleventh digit position, set Overflow FF. If second instruction digit is a minus sign, overflow sets Stop FF.	

INSTRUCTION	DESCRIPTION	FT
A F m	(m) ⟶ rX; (rX) + (rA) ⟶ rA	
1.	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB - OEC.	429
	Operate HSB - AOC.	428
	Set rM Read FF, set M1 Cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rX.	126
	Operate rX, clear gate.	120
	Operate extract circuit in rF.*	193
	Set MTO.	825
	Step PC, Set TO.	214
	*Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.	
TO	Compare (rA) and (rX).	NONE
2.	Operate adder for eleven-place addition.*	160
	Operate adder OE and sum comparison checkers.	435
	Connect rX to HSB.	125
	Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA (Transfer to rA ends at t12 of TO).	109
	Supply EP.	206
	*If decimal carry occurs from eleventh digit position, set Overflow FF.	

INSTRUCTION	DESCRIPTION	FT
A H m	(m) → rX; (rA) + (rX) → rA; (rA) → m	
1.	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB - OEC.	429
	Operate HSB - AOC.	428
	Set rM Read FF, set M_1 Cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rX.	126
	Operate rX clear gate.	120
	Set MTO.	825
	Step PC, set TO.	214
TO	Compare (rA) and (rX).	NONE
2.	Operate adder for eleven-place addition.*	160
	Operate adder OE and sum comparison checkers.	435
	Connect rX to HSB.	125
	Connect HSB to adder sub input, rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer to rA ends at t12 of TO.)	109
	Step PC, set TO.	214
	*If decimal carry occurs from 11th digit position, set Overflow FF.	206+
	+ FT206 is present, but its effect is suppressed by FT214.	
TO		
3.	Operate rM address exceeded and preset checkers.	860
	Connect rA to HSB.	100
	Operate HSB - OEC.	429
	Operate HSB - AOC.	428
	Set rM Read FF, set M_1 Cores.	826
	Develop Staticize Pulse.	823
	Set MTO.	825
	Supply EP.	206

INSTRUCTION	DESCRIPTION	FT
B 0 m	(m) → rA, rX.	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB - OEC.	429
	Operate HSB - AOC.	428
	Set rM Read FF, set M_1 Cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rA.	105
	Operate rA clear gate.	101
	Connect HSB to rX.	126
	Operate rX clear gate.	120
	Set MTO.	825
	Supply EP.	206
B F m	(m) → rA, rX.	
	Operate rM address exceeded and preset checkers.	860
	Preset BCM to RM.	827
	Operate HSB - OEC.	429
	Operate HSB - AOC.	428
	Set rM Read FF, set M_1 Cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate Extract Circuit in rF.*	193
	Connect HSB to rA.	105
	Operate rA clear gate.	101
	Connect HSB to rX.	126
	Operate rX clear gate.	120
	Set MTO.	825
	Supply EP.	206
	*Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.	

INSTRUCTION	DESCRIPTION	FT
C O m	(rA) → m; Z → rA	
	Operate rM address exceeded and preset checkers.	860
	Connect rA to HSB.	100
	Operate HSB - OEC.	429
	Operate HSB - AOC.	428
	Set rM Read FF, set M_1 Cores.	826
	Develop Staticize Pulse.	823
	Operate rA clear gate.	101
	Connect CU (000000 000000) to rA.	108
	Set MTO.	825
	Supply EP.	206
D O m	(m) → rA; (rA) ÷ (rL) → rA rounded, rX unrounded	
1.	Operate rM address exceeded and preset checker.	860
	Preset BCM to RM.	827
	Operate HSB - OEC.	429
	Operate HSB - AOC.	428
	Set rM Read FF, set M_1 Cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rA.	105
	Operate rA clear gate.	101
	Delete rX input to comparator, connect HSB.*	152
	Delete rA input to comparator, connect rL.*	151
	Preset BC-120 in MQC to non-complement position, thus alerting the non-complementing gates between MQC and MQC-FT. Clear MQC to decimal zero.	138
	Set MTO.	825
	Step PC, set TO.	214
	*Sign comparison is performed between (rA) and (rL).	

INSTRUCTION	DESCRIPTION	FT
D O m TO		
2.	Retain results of sign comparison in comparator. Operate rA clear gate. Operate rA left shift path (including sign).* Insert decimal zero in LSD position of rA. Set Repeat FF. Step PC, set TO. *Shifting (rA) left deletes sign digit.	159 101 103 171 226 214
TO		
3.	Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to HSB. Transfer (rL) to HSB, replacing sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop FF's after each time on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input clearing rA and transferring sum from adder to rA. Gate non-complement output of BC-120 as S1X signal to operate the complementer in adder sub, thus (rL) are subtracted from (rA). Gate non-complement output of BC-120 to operate Improper Division Detector in MQC.* Step MQC at t2 following each subtraction until the Through-Zero signal is developed, at which time generate OR CYCLE.# If rA or rX comp error occurs, set TO at following t1. *If rL ≥ rA, Improper Division occurs at t2 of the eleventh minor cycle of PC-3. #The Through-Zero signal indicates that the subtraction produced a negative remainder, since no decimal carry occurred from the twelfth-digit position. At the beginning of the OR CYCLE, the MQC-FT will contain a digit equal to the number of subtractions performed minus the one which produced the Through-Zero signal.	159 714 435 188 109 145 246

INSTRUCTION	DESCRIPTION	FT
D 0 m	Delete functions of FT109, except HSB to adder sub input. Inhibit the transfer of (rL) to HSB.	IER-OR+1 IER-OR+2
OR CYCLE	Delete functions of FT435. Operate rA and rX clear gates. Operate rX left shift path. Transfer quotient digit from MQC-FT to LSD position of rX. Clear MQC to decimal zero. Step BC-120 to alert the complement gates connecting the MQC and MQC-FT. (MQC-FT now reads nines complement of MQC.) Step PC at end of OR-CYCLE. Operate rA left shift path inserting a decimal zero in the LSD position Inhibit alerting signal to complementer and the stepping signal to the MQC. NOTE: Those FT signals present on PC-3 are also present during the OR CYCLE, performing the same functions except as noted above.	IER-OR+3 IER-OR-2 OR-1 OR-2 OR+1
4.	Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to HSB. Transfer (rL) to HSB, replacing sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop FF's after each Time-on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. Step MQC at t2 following each addition, until the Through-Zero signal is developed, at which time, generate OR CYCLE.* If rA or rX comp error occurs, set TO at following t1. *The Through-Zero signal indicates that the addition produced a positive number, since a decimal carry occurred from the twelfth digit position. At the beginning of the OR CYCLE, the MQC will contain a digit equal to the number of additions performed, minus the one which produced the Through-Zero signal, and the MQC-FT will contain the nines complement of this digit.	159 714 435 188 109 145 246

INSTRUCTION	DESCRIPTION	FT
D O m 5 thru 13	All OR CYCLES are identical. All odd PC-Steps are identical to PC-3. All even PC-Steps are identical to PC-4. Initially the divisor, (rL), is subtracted from the shifted dividend, (rA), until the Through-Zero signal occurs, indicating that the remainder in rA is negative. During the OR CYCLE (rA) and (rX) are shifted left one digit position, a decimal zero is inserted into the LSD position of rA and the quotient digit from the MQC-FT is inserted into the LSD position of rX. (rL) is then added to (rA) until the Through-Zero signal occurs, in this case indicating that (rA) is again positive; and an OR CYCLE occurs. (rL) is thus alternately subtracted and added to (rA) as the quotient is built up in rX. Following each OR CYCLE, PC is advanced.	
14	Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checker. Connect rL to HSB; transfer (rL) to HSB, replacing sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop after each time on minor cycle; if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. Step MQC at t2 following each addition, except when Through-Zero signal is developed at which time generate OR CYCLE. If rA, or rX comp occurs, set TO at following t1. Reset Repeat FF at end of OR CYCLE. Set TO at end of OR CYCLE.	159 714 435 188 109 145 246 228 244
OR CYCLE	Same as previous OR CYCLES, except that in addition: Reset Repeat FF. Set TO.	 IER-OR-1 OR-1

INSTRUCTION	DESCRIPTION	FT
D 0 m TO		
15	Retain results of sign comparison in comparator.	159
	Operate adder for twelve-place addition.	714
	Operate adder OE and sum comparison checkers.	435
	Operate rA clear gate.*	101
	Connect rX to HSB.	125
	Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA.	109
	Connect CU (round-off, 000000 000005) to adder min input.	111
	Step PC, set TO.	214
	*Operating rA's clear gate destroys the divide remainder and, consequently, nothing is read from rA to the adder min input. Thus the results of the addition are (rX) + (round-off) ⟶ rA.	
TO		
16	Retain results of sign comparison in comparator.	159
	Operate rA clear gate.	101
	Operate right shift path of rA. Transfer sign from comparator to rA and rX.	106
	Operate rX clear gate.	120
	Operate right shift path of rX.	123
	Transfer sign from comparator to rA and rX, deleting the insertion of a decimal zero to rA.	161
	Supply EP.	206

INSTRUCTION	DESCRIPTION	FT
D F m	(m)⟶rA; (rA) ÷ (rL)⟶rA rounded, rX unrounded	
1.	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB - OEC.	429
	Operate HSB - AOC.	428
	Set rM Read FF, set M_1 Cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rA.	105
	Operate rA clear gate.	101
	Operate Extract Circuit in rF.*	193
	Delete rA input to comparator, connect rL.#	151
	Delete rX input to comparator, connect HSB.#	152
	Preset BC-120 in MQC to non-complement position, thereby alerting the non-complement gates between MQC and MQC-FT. Clear MQC to decimal zero.	138
	Set MTO.	825
	Step PC, set TO.	214
	*Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.	
	#Perform sign comparison between (rA) and (rL).	
TO		
2.	Retain results of sign comparison in comparator.	159
	Operate rA clear gate.	101
	Operate rA left shift path.*	103
	Insert decimal zero in LSD position of rA.	171
	Set Repeat FF.	226
	Step PC, set TO.	214
	*Shifting (rA) left deletes sign digit.	

INSTRUCTION	DESCRIPTION	FT
D F m TO 3.	Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to HSB. Transfer (rL) to HSB, replacing the sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop after each time on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. Gate non-complement output of BC-120 as S1X signal to operate the Complementer on adder sub input, thus (rL) is subtracted from (rA). Gate non-complement output of BC-120 to operate the Improper Division Detector in MQC.* Step MQC t2 following each subtraction, until the Through-Zero signal is developed, at which time generate OR CYCLE.# If rA or rX comp error occurs, set TO at following t1. *If (rL) ≤ (rA), Improper Division occurs at t2 of the eleventh minor cycle of PC-3. #The Through-Zero signal indicates that the subtraction produced a negative remainder, since no decimal carry occurred from the twelfth digit position. At the beginning of the OR CYCLE, the MQC-FT will contain a digit equal to the number of subtractions performed minus the one which produced the Through-Zero signal.	159 714 435 188 109 145 246
OR CYCLE	Delete Functions of FT109, except HSB to adder sub input. Inhibit the transfer of (rL) to HSB. Delete functions of FT435. Operate rA and rX clear gates. Operate rX left shift path. Transfer quotient digit from MQC-FT to LSD position of rX. Clear MQC to decimal zero. Step BC-120 to alert the complement gates connecting the MQC and MQC-FT. (MQC-FT now reads nines complement of MQC) Step PC at end of OR CYCLE. Operate rA left shift path, insert a decimal zero into the LSD position of (rA). Inhibit alerting signal to complementer and the stepping signal to the MQC. NOTE: Those FT signals present on PC-3 are also present during the OR CYCLE, performing the same functions except as noted above.	IER-OR+1 IER-OR+2 IER-OR+3 IER-OR-2 OR-1 OR-2 OR+1

INSTRUCTION	DESCRIPTION	FT
D F m		
4.	Retain results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to HSB. Transfer (rL) to HSB, replacing the sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop FF's after each Time-on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA, and transfer sum from adder to rA. Step MQC at t2 following each addition, until the Through-Zero signal is developed, at which time generate OR CYCLE.* If rA or rX comp error occurs, set TO at following t1. *The Through-Zero signal indicates that the addition produced a positive number, since a decimal carry occurred from the twelfth digit position. At the beginning of the OR CYCLE, the MQC will contain a digit equal to the number of additions performed, minus the one which produced the Through-Zero signal, and the MQC-FT will contain the nines complement of this digit.	159 714 435 188 109 145 246
5-13	All OR CYCLES are identical. All odd PC-Steps are identical to PC-3. All even PC-Steps are identical to PC-4. Initially the divisor, (rL), is subtracted from the shifted dividend, (rA), until the Through-Zero signal occurs, indicating that the remainder in rA is negative. During the OR CYCLE, (rA) and (rX) are shifted one digit position left, a decimal zero is inserted into the LSD position of rA and the quotient digit from the MQC-FT is inserted into the LSD position of rX. (rL) is then added to (rA) until the Through-Zero signal occurs, in this case indicating that (rA) is again positive, and an OR CYCLE occurs. (rL) is thus alternately subtracted and added to (rA) as the quotient is built up in rX. After each OR CYCLE, PC is stepped.	

INSTRUCTION	DESCRIPTION	FT
D F m		
14.	Retain results of sign comparison in comparator.	159
	Operate adder for twelve-place addition.	714
	Operate adder OE and sum comparison checker.	435
	Connect rL to HSB. Transfer (rL) to HSB, replacing the sign digit with a decimal zero. Step PC upon completion of OR CYCLE. Set TO and Stop FF's after each Time-on minor cycle if IOS is in "One Addition".	188
	Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA.	109
	Step MQC at t2 following each addition, until the Through-Zero signal is developed, at which time generate OR CYCLE.	145
	If rA or rX comp error occurs, set TO at following t1.	246
	Reset Repeat FF at end of OR CYCLE.	228
	Set TO at end of OR CYCLE.	244
OR CYCLE	Same as previous OR CYCLES, except that in addition:	
	Reset Repeat FF.	IER-OR-1
	Set TO.	OR-1
TO		
15.	Retain results of sign comparison in comparator.	159
	Operate adder for twelve-place addition.	714
	Operate adder OE and sum comparison checker.	435
	Operate rA clear gate.*	101
	Connect rX to HSB.	125
	Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA.	109
	Connect CU roundoff, (000000 000005) to adder min input.	111
	Step PC, set TO.	214
	*Operating rA's clear gate destroys the divide remainder and, consequently, nothing is read from rA to the adder min input. Thus the results of the addition are: (rX) + (round-off)⟶rA.	

INSTRUCTION	DESCRIPTION	FT
D F m TO 16	Retain results of sign comparison in comparator. Operate rA clear gate. Operate right shift path of rA. Transfer sign from comparator to rA and rX. Operate rX clear gate. Operate right shift path of rX. Transfer sign from comparator to rA and rX, deleting the insertion of a decimal zero to rA. Supply EP.	159 101 106 120 123 161
E O m	(rF) Odd digits extracts (m)→rA. Operate rM address exceeded and preset checker. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, Set M_1 Cores. Strobe rM sense amplifiers. Develop Serialize Pulse Connect HSB to rA. Operate rA clear gate. Operate extract circuit in rF.* Delete CU (000000 000000) input to extract circuit and connect rA.* Set MTO. Supply EP. *Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is deleted and the corresponding digit from rA is transferred to the HSB.	860 827 429 428 820 821 824 105 101 193 832 825 206

INSTRUCTION	DESCRIPTION	FT
E F m	(rF) Even Digits Extracts (m)→rA; (rA)→m	
1.	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rA.	105
	Operate rA clear gate.	101
	Operate extract circuit in rF.*	193
	Complement the operation of the extract circuit.*	831
	Delete CU (000000 000000) input to extract circuit and connect rA.	832
	Set MTO.	825
	Step PC, set TO.	214
		206+
	*Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary one, the digit from rM is read onto the HSB. If the LSB is a binary zero, the digit from rM is deleted and the corresponding digit from rA is transferred to HSB.	
	+ FT206 is present, but its effect is suppressed by FT214.	
TO		
2.	Operate rM address exceeded and preset checkers.	860
	Connect rA to HSB.	100
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, Set M_1 cores.	826
	Develop Staticize Pulse.	823
	Set MTO.	825
	Supply EP.	206
F 0 m	(m)→rF	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rF, and operate rF clear gate.	190
	Set MTO.	825
	Supply EP.	206

INSTRUCTION	DESCRIPTION	FT
G 0 m	(rF)→m	
	Operate rM address exceeded and preset checkers.	860
	Connect rF to HSB.	192
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores.	826
	Develop Staticize Pulse.	823
	Set MTO.	825
	Supply EP.	206
H 0 m	(rA)→m	
	Operate rM address exceeded and preset checkers.	860
	Connect rA to HSB.	100
	Operate HSB-OEC.	429
	Operate HSB-AOC	428
	Set rM Read FF, set M_1 cores.	826
	Develop Staticize Pulse.	823
	Set MTO.	825
	Supply EP.	206
I 0 m	(rL)→m	
	Operate rM address exceeded and preset checkers.	860
	Connect rL to HSB.	187
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1cores.	826
	Develop Staticize Pulse.	823
	Set MTO.	825
	Supply EP.	206
J 0 m	(rX)→m	
	Operate rM address exceeded and preset checkers.	860
	Connect rX to HSB.	125
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM read FF, set M_1 cores.	826
	Develop Staticize Pulse.	823
	Set MTO.	825
	Supply EP.	206

INSTRUCTIONS	DESCRIPTION	FT
K 0	(rA) → rL; Z → rA.	
	Connect rA to HSB.	100
	Operate rA clear Gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect HSB to rL, operating rL clear gate.	185
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Supply EP.	206
L 0 m	(m) → rL, rX	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rL, operate rL clear gate.	185
	Operate rX clear gate.	120
	Connect HSB to rX input gate.	126
	Supply EP.	206
	Set MTO.	825
L F m	(m) → rL, rX	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 Cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate extract circuit in rF.*	193
	Connect HSB to rL, operate rL clear gate.	185
	Operate rX clear gate.	120
	Connect HSB to rX.	126
	Set MTO.	825
	Supply EP.	206
	*Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.	

INSTRUCTION	DESCRIPTION	FT
M O m	(m) → rX; (rL) x (rX) → rA (rounded) 11 MSD rX 11 LSD	
1	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M_1 cores. Strobe rM sense amplifiers. Develop Serialize Pulse. Operate rA clear gate. Connect CU (000000 000000) to rA. Connect rL to adder sub input. Transfer (rL) to adder, replacing sign digit with a decimal zero. Connect rA to adder min input, clear rA, and read sum from the adder to rA. (Transfer ends at t12 of TO.)* Operate adder OE and sum comparison checkers. Connect HSB to rX. Operate rX clear gate. Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC and MQC-FT. Set MTO. Step PC, set TO. *If decimal carry occurs from eleventh digit position, set Overflow flip-flop.	860 827 429 428 820 821 824 101 108 110 113 435 126 120 139 825 214
TO		
2	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign digit with a decimal zero. Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO) Step PC, set TO.	714 435 110 113 214

INSTRUCTION	DESCRIPTION	FT
M O m		
TO		
3	Operate adder for twelve-place addition.	714
	Operate adder OE and sum comparison checkers.	435
	Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign digit with a decimal zero.	110
	Delete rA input to comparator and connect rL.*	151
	Connect rA to adder min input, clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.)	113
	Step PC, set TO.	214
	*rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and (rX), and the sign of the product is stored in the comparator.	
TO		
4.	Store results of sign comparison in comparator.	159
	Operate adder OE and sum comparison checkers.	435
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect rA to HSB	100
	Operate rA clear gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect HSB to rF, operate rF clear gate.	190
	Connect CU (050000 000000) to adder sub input. Transfer the LSD of (rX) to the MQC and set the nines complement of the digit into the MQC.	112
	Connect rA to adder min input, clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.)	113
	Operate right shift path in rX	123
	Operate rX clear gate.	120
	Set Repeat flip-flop.	226
	Step PC,set TO.	214
	NOTE: At the completion of PC-4, rA contains the roundoff, rL contains the multiplicand, rF contains three times the multiplicand, rX contains the multiplier shifted one digit right, the MQC contains the nines complement of LSD shifted out of rX, and the comparator contains the sign of the product. The sign position of rX is vacant.	

INSTRUCTION	DESCRIPTION	FT
M O m TO		
	Store results of sign comparison in comparator. Operate adder for twelve-place addition.	159 714
5	Operate adder OE and sum comparison checkers. Connect rL and rF to the ≥ 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in One Addition. Connect HSB to adder sub input, rA to adder min input, clear rA and transfer the sum from the adder to rA. Sample (MQC-FT). If digit is < 3, reset the ≥ 3 FF, which transfers (rL) to HSB, and supply one stepping pulse to MQC. If digit is ≥ 3, set the ≥3 FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit = 0, set IER and IER-OR FF's at following t_2. If rA or rX comp error occurs, set TO at following t_1. NOTE: At the beginning of the operation, the MQC-FT will contain the LSD from rX. If the digit is ≥ 3, three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the digit in the MQC-FT by three. If the digit in the MQC-FT is < 3, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in the MQC-FT by one. Successive additions occur until the digit in the MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	435 188 109 147

INSTRUCTION	DESCRIPTION	FT
M O m IER (PC-5)	Operate the right shift path of rA and insert a decimal zero into the sign position of (rA). Operate the right shift path of rX, transferring LSD of (rX) to the MQC distributor line. Operate rA and rX clear gates. Clear MQC to binary zero and set up the complement of the LSD from (rX) in the MQC. Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER-CYCLE. Inhibit the transfer of (rL) and the decimal zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the stepping of the MQC. Inhibit min input to the algebraic adder. (Delete the functions of FT109) Inhibit the adder OE and sum comparison checkers. (Delete the functions of FT435)	IER-6 IER-4 IER-OR-2 IER-3 IER-1 IER-OR+2 IER+1 IER-OR+1 IER-OR+3
6 through 13	Same as PC-5.	
14	Same as PC-5 except for one addition FT signal which is used to set TO at the end of the IER CYCLE.	244
TO		
15 PC 15 IER	Same as PC-5 except for four additional FT signals which are used during PC-15 IER CYCLE. Insert sign into sign position of (rA) and (rX). Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC. Reset Repeat FF. Supply EP.	 161 & IER -5 149 & IER-1 228 & IER-OR-1 215 & IER-2

INSTRUCTION	DESCRIPTION	FT
M F m	(m) → rX; (rL) x (rX) → rA (rounded) 11 MSD rX 11 LSD	
1	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate rA clear gate.	101
	Operate extract circuit in rF.*	193
	Connect CU (000000 000000) to rA.	108
	Connect rL to adder sub input, transfer (rL) to adder, replacing sign digit with a decimal zero.	110
	Connect rA to adder Min input, clear rA, and read the sum from the adder to rA. (Transfer ends at t12) +	113
	Operate adder OE and sum comparison checkers.	435
	Connect HSB to rX.	126
	Operate rX clear gate.	120
	Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC to the MQC-FT.	139
	Set MTO.	825
	Step PC, set TO.	214
	*Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.	
	+If decimal carry occurs from eleventh digit position, set Overflow flip-flop.	
TO		
2	Operate adder for twelve-place addition.	714
	Operate adder OE and sum comparison checkers.	435
	Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign digit with a decimal zero.	110
	Connect rA to adder min input, clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.)	113
	Step PC, set TO.	214

INSTRUCTION	DESCRIPTION	FT
M F m 3	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign digit with a decimal zero. Delete rA input to comparator, connect rL.* Connect rA to adder min input, clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.) Step PC, set TO. *rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and (rX), and the sign of the product is stored in the comparator.	714 435 110 151 113 214
TO 4	Store results of sign comparison in comparator. Operate adder OE and sum comparison checkers. Operate HSB-OEC. Operate HSB-AOC. Connect rA to HSB. Operate rA clear gate. Connect CU (000000 000000) to rA. Connect HSB to rF, operating rF Clear gate. Connect CU (050000 000000) to adder sub input. Transfer the LSD of (rX) to the MQC, setting the nines complement of the digit into the MQC. Connect rA to Min input, clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.) Operate right shift path in rX. Operate rX clear gate. Set Repeat flip-flop. Step PC, set TO. NOTE: At the completion of PC-4, rA contains the roundoff, rL contains the multiplicand, rF contains three times the multiplicand, rX contains the multiplier shifted one digit right, the MQC contains the nines complement of LSD shifted out of rX, and the comparator contains the sign of the product. The sign position of rX is vacant.	159 435 429 428 100 101 108 190 112 113 123 120 226 214

INSTRUCTION	DESCRIPTION	FT
M F m		
TO		
5	Store results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL and rF to the ≥ 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in"One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. Sample (MQC-FT). If digit is < 3, reset the ≥ 3 FF, which transfers (rL) to HSB, and supplies one stepping pulse to MQC. If digit is ≥ 3, set the ≥ 3 FF, which transfers (rF) to HSB, and supplies three stepping pulses to MQC. If digit is = 0, set IER and IER-OR FF's at following t2. If rA or rX comp error occurs, set TO at following t1. NOTE: At the beginning of the operation, the MQC-FT will contain the LSD from rX. If the digit is ≥ 3, three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the digit in MQC-FT by three. If the digit in MQC-FT is < 3, the multiplicand (rL) is added to the partial product in rA and MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in the MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	159 714 435 188 109 147 246
IER CYCLE	Operate the right shift path of ra and insert a decimal zero into the sign position of (rA). Operate the right shift path of rX transferring LSD of rX to the MQC distributor line. Operate rA and rX clear gates. Clear MQC to binary zero and set up the complement of the LSD from (rX) in the MQC. Transfer LSD of (rA) to the MSD position of rX and step PC at the end of the IER CYCLE. Inhibit the transfer of (rL) and the decimal zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the stepping of the MQC. Inhibit the min input of the algebraic adder. (Delete the functions of FT109) Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of FT435)	IER-6 IER-4 IER-OR-2 IER-3 IER-1 IER-OR+2 IER+1 IER-OR+1 IER-OR+3

INSTRUCTION	DESCRIPTION	FT
M F m 6 through 13	Same as PC-5.	
14	Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE.	244
TO		
15	Same as PC-5 except for four additional FT signals which are used during PC-15 IER CYCLE.	
PC 15	Insert sign into sign position of (rA) and (rX).	161 Plus
IER CYCLE	Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC.	149 Plus IER-1
	Reset Repeat FF.	228 Plus IER-OR-1
	Supply EP.	215 Plus IER-2
N O m	-(m) → rX; (rL) X (rX) → rA (rounded) 11 MSD's rX 11 LSD's	
1	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM	827
	Operate HSB-OEC	429
	Operate HSB-AOC	428
	Set rM Read FF, set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate rA clear gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect rL to adder sub input. Transfer (rL) to adder, replacing sign digit with a decimal zero	110
	Connect rA to adder min input. Clear rA and read the sum from the adder to rA. (Transfer ends at t12 of TO)*	113
	Operate adder OE and sum comparison checkers.	435
	Connect HSB to rX, via sign reversal gates.+	153
	Operate rX clear gate.	120
	Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC to MQC-FT.	139
	Set MTO.	825
	Step PC, set TO.	214
	*If decimal carry occurs from eleventh digit position, set Overflow flip-flop.	
	+The sign reversal gates complement the LSB and check pulse of the sign digit during transfer to rX.	

INSTRUCTION N O m	DESCRIPTION	FT
TO		
2	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing sign digit with a decimal zero. Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.) Step PC, set TO.	714 435 110 113 214
TO		
3	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign digit with a decimal zero. Delete rA input to comparator, connect rL.* Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.) Step PC, set TO. *rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and (rX), and the sign of the product is stored in the comparator.	714 435 110 151 113 214

INSTRUCTION	DESCRIPTION	FT
N O m		
TO		
4	Store results of sign comparison in comparator.	159
	Operate adder OE and sum comparison checkers	435
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect rA to HSB.	100
	Operate rA clear gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect HSB to rF, operate rF clear gate.	190
	Connect CU (050000 000000) to adder sub input. Transfer the LSD of (rX) to the MQC and set up the nines complement of the digit into the MQC	112
	Connect rA to min input of the adder. Clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.)	113
	Operate right shift path in rX.	123
	Operate rX clear gate.	120
	Set Repeat flip-flop.	226
	Step PC, set TO.	214
	NOTE: At the completion of PC-4, rA contains the roundoff. rL contains the multiplicand, rF contains three times the absolute value of the multiplicand, rX contains the multiplier shifted one digit right, the MQC contains the nines complement of LSD shifted out of rX, and the comparator contains the sign of the product. The sign position of rX is vacant.	

INSTRUCTION	DESCRIPTION	FT
N O m TO		
5	Store results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers Connect rL and rF to the ≥ 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. Sample (MQC-FT). If digit is < 3, reset the ≥ 3 FF, which transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is ≥ 3, set the ≥ 3 FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit is = 0, set IER and IER-OR FF's at following t2. If rA or rX comp error occurs, set TO at following t1. NOTE: At the beginning of the operation, the MQC-FT will contain the LSD from rX. If the digit is ≥ 3, three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the digit in MQC-FT by three. If the digit in the MQC-FT is < 3, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	159 714 435 188 109 147 246

INSTRUCTION	DESCRIPTION	FT
N O m IER CYCLE (PC-5)	Operate the right shift path of rA and insert a decimal zero into the sign position of (rA). Operate the right shift path of rX, transferring LSD of rX to the MQC distributor line. Operate rA and rX clear gates. Clear MQC to binary zero and set up the complement of the LSD from rX in the MQC. Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. Inhibit the transfer of (rL) and the decimal zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the stepping of the MQC. Inhibit the min input to the algebraic adder. (Delete the functions of FT109) Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of FT435.)	IER-6 IER-4 IER-OR-2 IER-3 IER-1 IER-OR+2 IER + 1 IER-OR+1 IER-OR+3
6 through 13	Same as PC-5.	
14	Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE.	244
TO		
15	Same as PC-5 except for four additional FT signals which are used during PC-15 IER CYCLE.	
PC 15 IER CYCLE	Insert sign into sign position of (rA) and (rX). Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC. Reset Repeat FF. Supply EP.	161 plus IER-5 149 plus IER-1 228 plus IER-OR-1 215-plus IER-2

INSTRUCTION N F m	DESCRIPTION	FT
	-(m)→rX; (rL) X (rX)→rA (rounded) 11 MSD's rX 11 LSD's	
1	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM	827
	Operate HSB-OEC	429
	Operate HSB-AOC	428
	Set rM Read FF, set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate rA clear gate	101
	Connect CU (000000 000000) to rA.	108
	Connect rL to adder sub input, transfer (rL) to adder, replacing sign digit with a decimal zero.	110
	Connect rA to adder min input. Clear rA, and read the sum from the adder to rA. (Transfer ends at t12 of T0.)*	113
	Operate adder OE and sum comparison checkers	435
	Operate extract control circuit in rF.+	193
	Connect HSB to rX, via sign reversal gates.#	153
	Operate rX clear gate.	120
	Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC to MQC-FT.	139
	Set MT0.	825
	Step PC, set T0.	214
	*If decimal carry occurs from eleventh digit position, set Overflow flip-flop.	
	#The sign reversal gates complement the LSB and check pulse of the sign digit during transfer to rX.	
	+Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.	

INSTRUCTION N F m	DESCRIPTION	FT
TO		
2	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing sign with a decimal zero. Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.) Step PC, set TO.	714 435 110 113 214
TO		
3	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign with a decimal zero. Delete rA input to comparator, connect rL.* Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.) Step PC, set TO. *rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and (rX), and the sign of the product is stored in the comparator.	714 435 110 151 113 214

INSTRUCTION N F m	DESCRIPTION	FT
TO		
4	Store results of sign comparison in comparator.	159
	Operate adder OE and sum comparison checkers.	435
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect rA to HSB.	100
	Operate rA clear gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect HSB to rF, operate rF clear gate.	190
	Connect CU (050000 000000) to adder sub input. Transfer the LSD of (rX) to the MQC, set up the nines complement of the digit into the MQC.	112
	Connect rA to min input of the adder. Clear rA, and read sum from adder to rA. (Transfer ends at t12 of TO.)	113
	Operate right shift path in rX.	123
	Operate rX clear gate.	120
	Set Repeat flip-flop.	226
	Step PC, set TO.	214
	NOTE: At the completion of PC-4, rA contains the roundoff, rL contains the multiplicand, rF contains three times the absolute value of the multiplicand, rX contains the multiplier shifted one digit right, the MQC contains the nines complement of LSD shifted out of rX, and the comparator contains the sign of the product. The sign position of rX is vacant.	

INSTRUCTION N F m TO	DESCRIPTION	FT
5	Store results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL and rF to the ≥ 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign digit with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS, is in"One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. Sample (MQC-FT). If digit is < 3, reset ≥ 3 FF, which transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is ≥ 3, set the ≥ 3 FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit is = 0, set IER and IER-OR FF's at following t2. If rA or rX comp error occurs, set TO at following t1. NOTE: At the beginning of the operation, the MQC-FT will contain the LSD from rX. If the digit is ≥3, three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the MQC-FT by three. If the digit in MQC-FT is < 3, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	159 714 435 188 109 147 246

INSTRUCTION	DESCRIPTION	FT
N F m IER CYCLE (PC-5)	Operate the right shift path of rA and insert a decimal zero into the sign position. Operate the right shift path of rX transferring LSD of rX to the MQC distributor line. Operate rA and rX clear gates. Clear MQC to binary zero and set up the complement of the LSD from (rX) in the MQC. Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. Inhibit the transfer of (rL) and the decimal zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the stepping of the MQC. Inhibit the min input to the algebraic adder. (Delete the functions of FT109) Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of (FT435.)	IER-6 IER-4 IER-OR-2 IER-3 IER-1 IER-OR+2 IER+1 IER-OR+1 IER-OR+3
6 Through 13	Same as PC-5.	
14	Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE.	244
TO		
15	Same as PC-5 except for four additional FT signals which are used during PC-15 IER CYCLE.	
PC-15 IER CYCLE	Insert sign into the sign position of rA and rX. Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC. Reset Repeat FF. Supply EP.	161 Plus IER-5 149 Plus IER-1 228 Plus IER-OR-1 215 Plus IER-2

INSTRUCTION	DESCRIPTION	FT
P O m	(m) → rX; (rL) X (rX) → rA = 11 MSD's, rX = 11 LSD's	
1	Operate rM Address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-AOC.	428
	Operate HSB-OEC.	429
	Set rM Read FF, set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate rA clear gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect rL to adder sub input, transfer (rL) to adder and replace sign digit of (rL) with a decimal zero.	110
	Connect rA to adder min input, Clear rA and read sum from adder to rA. (Transfer ends at t12 of TO.)*	113
	Operate adder OE and sum comparison checkers.	435
	Connect HSB to rX.	126
	Operate rX clear gate.	120
	Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC and MQC-FT.	139
	Set MTO.	825
	Step PC, set TO.	214
	*If decimal carry occurs from the eleventh digit position, set Overflow FF.	
TO		
2	Operate adder for twelve-place addition.	714
	Operate adder OE and sum comparison checkers.	435
	Connect rL to sub input of adder, transfer (rL) to adder, replacing the sign digit with a decimal zero.	110
	Connect rA to adder min input. Clear rA and read sum from adder to rA.	113
	Step PC, set TO.	214

INSTRUCTION P O m TO	DESCRIPTION	FT
3	Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL to sub input of adder, transfer (rL) to adder, replacing the sign digit with a decimal zero. Delete rA input to comparator and connect rL.* Connect rA to adder min input. Clear rA and read sum from adder to rA. Step PC, set TO. *rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and (rX), and the sign of the product is stored in the comparator.	714 435 110 151 113 214
TO		
4	Store results of sign comparison in comparator. Operate HSB-OEC. Operate HSB-AOC. Connect rA to HSB. Operate rA clear gate. Connect CU (000000 000000) to rA. Connect HSB to rF and operate rF clear gate. Connect CU (050000 000000) to adder sub input. Transfer the LSD of (rX) to the MQC and set up the nines complement of the digit into the MQC. Operate right shift path in rX. Operate rX clear gate. Set Repeat FF. Step PC, set TO. NOTE: At the completion of PC-4, rA contains decimal zeros, rL contains the multiplicand, rF contains three times the multiplicand, and rX contains the multiplier shifted one digit right, the MQC contains the nines complement of the LSD shifted out of rX, and the comparator contains the sign of the product. The sign position of rX is vacant.	159 429 428 100 101 108 190 112 123 120 226 214

INSTRUCTION	DESCRIPTION	FT
P O m TO PC-5	Store result of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL and rF to the ≥ 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and Stop FF's at end of each Time-on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. Sample (MQC-FT). If digit is < 3, reset the ≥ 3 FF, which transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is ≥ 3, set the ≥ 3 FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit = 0, set IER and IER OR FF's at following t2. If rA or rX comp. error occurs, set to FF at following t1. NOTE: At the beginning of the operation, the MQC-FT will contain the LSD from rX. If the digit is ≥ 3, three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the digit in the MQC-FT by three. If the digit in the MQC-FT is < 3, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in the MQC-FT by one. Successive additions occur until the digit in the MQC-FT is reduced to zero, at which time the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	159 714 435 188 109 147 246
IER PC-5	Operate the right shift path of rA and insert a decimal zero into the sign position. Operate the right shift path of rX, including the sign, transfer LSD of rX to the MQC distributor line. Operate rA and rX clear gates. Clear MQC to binary zero and set up the complement of the LSD from rX in the MQC. Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. Inhibit the transfer of (rL) and the decimal zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the stepping of the MQC. Inhibit the min input to the algebraic adder. (Delete the functions of FT109) Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of FT435.)	IER-6 IER-4 IER-OR-2 IER-3 IER-1 IER-OR+2 IER+1 IER-OR+1 IER-OR+3

INSTRUCTION	DESCRIPTION	FT
P O m 6 Through 13	Same as PC-5.	
PC-14	Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE.	244
IER	Insert sign into the sign position of (rA) and (rX).	161 Plus IER-5
PC-15	Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC.	149 Plus IER-1
	Reset Repeat FF.	228 Plus IER-OR-1
	Supply EP.	215 Plus IER-2
P F m	(m) ⟶ rX; (rL) X (rX) ⟶ rA, 11 MSD's rX, 11 LSD's	
1	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate rA clear gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect rL to adder sub input, transfer (rL) to adder, replacing sign digit with a decimal zero.	110
	Connect rA to adder min input. Clear rA, and read the sum from the adder to rA. (Transfer ends at t12 of TO.)*	113
	Operate adder OE and sum comparison checkers.	435
	Operate extract control circuit in rF.+	193
	Connect HSB to rX.	126
	Operate rX clear gate.	120
	Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC to the MQC-FT.	139
	Set MTO.	825
	Step PC, set TO.	214
	*If decimal carry occurs from eleventh digit position, set Overflow flip-flop.	
	+Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.	

INSTRUCTION	DESCRIPTION	FT
P F m	Operate adder for twelve-place addition.	714
	Operate adder OE and sum comparison checkers	435
TO	Connect rL to sub input of adder. Transfer (rL) to adder, replacing sign digit with a	
2	decimal zero.	110
	Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at	
	t12 of TO.)	113
	Step PC, set TO.	214
TO		
3	Operate adder for twelve-place addition.	714
	Operate adder OE and sum comparison checkers.	435
	Connect rL to sub input of adder. Transfer (rL) to adder, replacing the sign digit with	
	a decimal zero.	110
	Delete rA input to comparator and connect rL.*	151
	Connect rA to adder min input. Clear rA, and read sum from adder to rA. (Transfer ends at	
	t12 of TO.)	113
	Step PC, set TO.	214
	*rX is connected to the comparator via a direct path. A sign comparison is performed between (rL) and (rX), and the sign of the product is stored in the comparator.	
TO		
4	Store results of sign comparison in computer.	159
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect rA to HSB.	100
	Operate rA clear gate.	101
	Connect CU (000000 000000) to rA.	108
	Connect HSB to rF, operating rF clear gate.	190
	Connect CU (050000 000000) to adder sub input. Transfer the LSD of (rX) to the MQC and set up the	
	nines complement of the digit into the MQC.	112
	Operate right shift path in rX.	123
	Operate rX clear gate.	120
	Set Repeat flip-flop.	226
	Step PC, set TO.	214
	NOTE: At the completion of PC-4, rA contains decimal zeros, rL contains the multiplicand, rF contains three times the multiplicand, rX contains the multiplier shifted one digit right, the MQC contains the nines complement of the LSD shifted out of rX, the Comparator contains the sign of the product, and the sign position of rX is vacant.	

INSTRUCTION	DESCRIPTION	FT
P F m TO 5	Store results of sign comparison in comparator. Operate adder for twelve-place addition. Operate adder OE and sum comparison checkers. Connect rL and rF to the ≥ 3 FF control circuits. Transfer of (rL) to the HSB and replace the sign with a decimal zero during the transfer. Step PC at end of each IER CYCLE. Set TO and stop FF's at end of each Time-on minor cycle if IOS is in "One Addition". Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer the sum from the adder to rA. Sample (MQC-FT). If digit is < 3, reset ≥ 3 FF, which transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is ≥ 3, set the ≥ 3 FF, which transfers (rF) to HSB and supplies three stepping pulses to MQC. If digit is = 0, set IER and IER-OR FF at following t2. If rA or rX comp error occurs, set TO FF at following t1. NOTE: At the beginning of the operation, the MQC-FT will contain the LSD from rX. If the digit is ≥ 3, three times the multiplicand (rF) is added to the partial product in rA, and the MQC is stepped three times, thus reducing the MQC-FT by three. If the digit in MQC-FT is < 3, the multiplicand (rL) is added to the partial product in rA and the MQC is stepped once, thus reducing the digit in MQC-FT by one. Successive additions occur until the digit in MQC-FT is reduced to zero, at which time the IER CYCLE is generated. At the beginning of the IER CYCLE, rA will contain (rL) times the original LSD of (rX).	159 714 435 188 109 147 246
P F m IER CYCLE (PC-5)	Operate the right shift path of rA, inserting a decimal zero into the sign position. Operate the right shift path of rX, transferring LSD of rX to the MQC distributor line. Operate rA and rX clear gates. Clear MQC to binary zero and set up the complement of the LSD from (rX) in the MQC. Transfer LSD of (rA) to the MSD position of rX, step PC at the end of the IER CYCLE. Inhibit the transfer of (rL), and the decimal zero for the sign position of (rL) to the HSB. Disconnect rF from the HSB and inhibit the stepping of the MQC. Inhibit the min input to the algebraic adder. (Delete the functions of FT109) Inhibit the adder odd-even and the adder sum comparison checkers. (Delete the functions of FT435.)	IER-6 IER-4 IER-OR-2 IER-3 IER-1 IER-OR+2 IER+1 IER-OR+1 IER-OR+3

INSTRUCTION	DESCRIPTION	FT
P F M 6 through 13	Same as PC-5.	
14	Same as PC-5 except for one additional FT signal which is used to set TO at the end of the IER CYCLE.	244
TO		
15	Same as PC-5 except for four additional FT signals which are used during PC-15 IER CYCLE.	
PC-15 IER CYCLE	Insert sign in sign position of (rA), (rX). Inhibit the generation of a second IER CYCLE in case a decimal zero is set up in the MQC. Reset Repeat FF. Supply EP.	161 Plus IER 5 149 Plus IER-1 228 Plus IER-OR-1 215 Plus IER 2
Q n m	If (rA) = (rL), Transfer control⟶ m.	
1	Operate HSB-OEC. Operate HSB-AOC. Connect rL to HSB. Eanble comparator to perform equality comparison.* Delete rX input to comparator and connect HSB. If 2nd Instruction Digit "n" equals Conditional Transfer Breakpoint Selector setting, pass t1 to set Stop FF. Step PC, set TO. *If (rA) = (rL), the Conditional Transfer FF is set at t5 of PC-2 TO.	429 428 187 156 152 236 214
TO		
2	Retain results of comparison in comparator. Operate HSB-OEC. Operate HSB-AOC. Connect CR and CU (000000 00) to HSB.* If Conditional Transfer FF is set, connect HSB to CC and operate CC clear gate. Supply EP. *The four LSD's of (CR) are merged with eight decimal zeros from CU to make the complete word which is transferred to the HSB.	159 429 428 200 209 206

INSTRUCTION	DESCRIPTION	FT
R 0 m	(000000 UO(CC))⟶ m	
	Operate rM address exceeded and preset checkers.	860
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect CC and CU (000000 UO) to HSB.*	245
	Set rM Read FF, set M_1 cores.	826
	Develop Staticize Pulse.	823
	Set MTO.	825
	Supply EP.	206
	*The four LSD's of (CC) are merged with (000000 UO) from the CU to make the complete word which is transferred to the HSB.	
S 0 m	-(m)⟶ rX; (rX) + (rA)⟶ rA	
1	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rX via sign reversal gates.*	153
	Operate rX clear gate.	120
	Set MTO.	825
	Step PC, set TO.	214
	*The sign reversal gates complement the LSB and check pulse of the sign during transfer to rX.	
TO	Compare (rA) and (rX).	None
2	Operate adder for eleven place addition.*	160
	Operate adder OE and sum comparison checkers.	435
	Connect rX to HSB.	125
	Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA.	109
	Supply EP.	
	*If decimal carry occurs from eleventh digit position, set Overflow FF. If Second Instruction Digit is a minus sign, overflow sets Stop FF.	

INSTRUCTION	DESCRIPTION	FT
S F m	-(m) → rX; (rX) + (rA) → rA.	
1	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Connect HSB to rX via sign reversal gates.+	153
	Operate rX clear gate.	120
	Operate extract circuit in rF.*	193
	Set MTO.	825
	Step PC, set TO.	214
	*Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.	
	+The sign reversal gates complement the LSB and check pulse of the sign during transfer to rX.	
TO	Compare (rA) and (rX).	None
2	Operate adder for eleven place addition.*	160
	Operate adder OE and sum comparison checkers.	435
	Connect rX to HSB.	125
	Connect HSB to adder sub input and rA to adder min input. Clear rA and transfer sum from adder to rA.	109
	Supply EP.	206
	*If decimal carry occurs from eleventh digit position, set Overflow FF.	

INSTRUCTION	DESCRIPTION	FT
S H m	-(m) ⟶ rX; (rX) + (rA) ⟶ rA ⟶ m	
1	Operate rM address exceeded and preset checkers. Set BCM to RM. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M_1 cores. Strobe rM sense amplifiers. Develop Serial Pulse. Connect HSB to rX via sign reversal gates.* Operate rX clear gate. Set MTO. Step PC, set TO. *The sign reversal gates complement the LSB and check pulse of the sign during transfer to rX.	860 827 429 428 820 821 824 153 120 825 214
TO	Compare (rA) and (rX).	None
S H m		
2	Operate adder for eleven place addition.* Operate adder OE and sum comparison checkers. Connect rX to HSB. Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA. Step PC, set TO. *If decimal carry occurs from eleventh digit position, set Overflow FF. +FT206 is present, but its effect is suppressed by FT214.	160 435 125 109 214 206+
TO		
S H m		
3	Operate rM address exceeded and preset checkers. Connect rA to HSB. Operate HSB-OEC. Operate HSB-AOC. Set rM Read FF, set M_1 cores. Develop Staticize Pulse. Set MTO. Supply EP.	860 100 429 428 826 823 825 206

INSTRUCTION	DESCRIPTION	FT
T n m	If (rA) > (rL), Transfer control to m.	
1	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect rL to HSB.	187
	Set up comparator to perform algebraic comparison.*	172
	Delete rX input to comparator and connect HSB.	152
	If 2nd Instruction Digit "n" equals Conditional Transfer Breakpoint Selector setting, pass t1 to set Stop FF.	236
	Step PC, set TO.	214
	*If (rA) > (rL), the Conditional Transfer FF is set at t5 of PC-2 TO.	
TO		
T n m		
2	Retain results of comparison in comparator.	159
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect CR and CU (000000 00) to HSB.*	200
	If Conditional Transfer FF is set, connect HSB to CC and operate CC clear gate.	209
	Supply EP.	206
	*The four LSD's of (CR) are merged with eight decimal zeros from CU to make the complete word which is transferred to the HSB.	
U 0 m	Transfer control to m	
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect CR and CU (000000 00) to HSB.	200
	Connect HSB to CC, operating CC clear gate.	208
	Supply EP.	206

INSTRUCTION	DESCRIPTION	FT
V n m	(m), (m+1) . . . . (m+n-1) → rW	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores.	820
	Preset rZW units counter to elevens complement of the 2nd Instruction Digit. When the rZW units counter reads zero, gate a t59 to set MTO.*+#	817
	Read and restore rZW simultaneously with the reading and restoring of rM. When MTO is set, supply EP.	818
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Step rM counters and rZW units counter once each minor cycle until rZW units counter reads zero.	833
	Supply EP.	206
	*If 2nd Instruction Digit is a zero and if compatibility switch on SC is set to Univac II, treat instruction as a Skip.	
	+If Compatibility switch is set to Univac I, the rZW units counter is unconditionally set to nine.	
	#The "Tens" 7 or W line is always up except during the Y or Z instructions.	

INSTRUCTION	DESCRIPTION	FT
W n m	(rW) → m, m + 1 ..... m+n-1	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores.	820
	Preset rZW units counter to elevens complement of the 2nd Instruction Digit. When the rZW units counter reads zero, gate a t59 to set MTO.*+#	817
	Read and restore rZW simultaneously with the reading and restoring of rM. When MTO is set, supply EP.	818
	Strobe rZW sense amplifiers.	819
	Develop Serialize Pulse.	824
	Step rM counters and rZW units counter once each minor cycle until rZW units counter reads zero.	833
	Supply EP.	206
	*If 2nd Instruction Digit is a zero and if Compatibility switch on SC is set to Univac II, treat instruction as a Skip.	
	+If Compatibility switch is set to Univac I the rZW units counter is unconditionally set to nine.	
	#The "Tens" 7 or W line is always up except during the Y or Z instructions.	
X 0 m	(rA) + (rX) → rA	
TO	Compare (rA) and (rX).	None
	Operate adder for eleven place addition.*	160
	Operate adder OE and sum comparison checkers.	435
	Connect rX to HSB.	125
	Connect HSB to adder sub input, rA to adder min input. Clear rA and transfer sum from adder to rA.	109
	Supply EP.	206
	*If decimal carry occurs from eleventh digit position, set Overflow FF. If second instruction digit is a minus sign, overflow sets Stop FF.	

INSTRUCTION	DESCRIPTION	FT
Y n m	(m), (m+1) ..... (m+10n - 1) → rZ	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC	428
	Set rM Read FF, set M_1 cores.	820
	Preset rZW tens counter to elevens complement of the 2nd Instruction Digit. Preset rZW units counter to one.	
	When the rZW tens and units counters read zero, gate a t59 to set MTO. *+	816
	Read and restore rZW simultaneously with the reading and restoring of rM. When MTO is set, supply EP.	818
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Step rM counters and rZW units counter once each minor cycle. When the rZW units counter passes trhough zero it steps the rZW tens counter.	833
	Supply EP.	206
	*If 2nd Instruction Digit is a 7, 8, 9, or 0, and if Compatibility switch on SC is set to Univac II, treat instruction as a Skip.	
	+If Compatibility switch is set to Univac I, the rZW tens counter is preset to zero.	
Z n m	(rZ) → m, m+1 ..... m+10n-1	
	Operate rM address exceeded and preset checkers.	860
	Set BCM to RM.	827
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rM Read FF, set M_1 cores.	820
	Preset rZW tens counter to elevens complement of the 2nd Instruction Digit. Preset rZW units counter to one.	
	When the rZW tens and units counters read zero, gate a t59 to set MTO. *+	816
	Read and restore rZW simultaneously with the reading and restoring of rM. When MTO is set, supply EP.	818
	Strobe rZW sense amplifiers.	819
	Develop Serialize Pulse.	824
	Step rM counters and rZW units counter once each minor cycle. When the rZW units counter passes through zero it steps the rZW tens counter.	833
	Supply EP.	206
	*If 2nd Instruction Digit is a 7, 8, 9, or 0, and if Compatibility switch on SC is set to Univac II, treat instruction as a Skip.	
	+If Compatibility switch is set to Univac I, the rZW tens counter is preset to zero.	

INSTRUCTION	DESCRIPTION	FT
.n m	Shift rA right, with sign, n places	
All	Preset rZW units counter to the elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO.	817
	Operate rA clear gate.	101
	Operate right shift path of rA and insert a decimal zero into the sign position.*	106
	Step rZW and rM counters once each minor cycle until rZW units counter reads zero.	833
	Step PC once per minor cycle. +	213
	When MTO is set, supply EP at following t1.	818
	*rA shifts one digit right during each minor cycle of Time-on.	
	+If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting the FT Intermediate Checker FF, and TO.	
-n m	Shift rA right, without sign, n places	
All	Preset rZW units counter to the elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO.	817
	Operate rA clear gate, except for sign position.	170
	Operate right shift path of rA and insert a decimal zero into the (MSD) position.*	107
	Step rZW and rM counters once each minor cycle until rZW units counter reads zero.	833
	Step PC once each minor cycle. +	213
	When MTO is set, supply EP and set TO at following t1.	818
	*rA shifts one digit right during each minor cycle of Time-on.	
	+If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting the FT Intermediate Checker FF and TO.	

INSTRUCTION	DESCRIPTION	FT
;n m	Shift rA left, with sign, n places	
All	Preset rZW units counter to elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO.	817
	Operate rA clear gate.	101
	Operate left shift path of rA. *	103
	Insert decimal zero into LSD position of (rA).	171
	Step rZW and rM counters once each minor cycle until rZW units counter reads zero.	833
	Step PC once each minor cycle. +	213
	When MTO is set, supply EP and set TO at following t1.	818
	*rA shifts one digit left during each minor cycle of Time-on.	
	+If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting FT Intermediate Checker FF and TO.	
0 n m	Shift rA left, without sign, n places	
All	Preset rZW units counter to elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO.	817
	Operate rA clear gate, except for sign position.	170
	Operate left shift path of rA. *	104
	Insert decimal zero into LSD position of (rA).	171
	Step rZW and rM counters once each minor cycle until rZW units counter reads zero.	833
	Step PC once each minor cycle. +	213
	When MTO is set, supply EP at following t1.	818
	*rA shifts one digit left during each minor cycle of Time-on.	
	+If PC is advanced in excess of thirteen, an Overshift signal is developed which stalls machine operation by setting FT Intermediate Checker FF and TO.	

INSTRUCTION	DESCRIPTION	FT
0 0 m	Skip instruction (Supply Ending Pulse and proceed to next instruction) Supply EP.	 206
0 m	Stop computation if Breakpoint switch on SC is depressed Set Stop FF if Breakpoint switch is depressed. Supply EP.	 217 206
9 0 m	Stop computation Set Stop FF. Supply EP.	 218 206
1 n m	60 words from tape to rI, forward	
1	Gate nS (Servo Selector) signal from second Instruction Digit to determine if Uniservo desired will pass interlock. Gate, FIR, BIR or FIR-BIR to determine if computer will pass interlock to start read operation. ≠ + If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At following t1 generate IRP. * Gate IRP as Sequence I Preset. + Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms. * IRP is used to: 1. Step PC. 2. Set TO. 3. Supply set pulse to Direction Memory. 4. Set Reversal Memory if BIR was returned from Uniservo. 5. Reset Interlock Release FF. 6. Supply Sequence I Preset. ≠ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.)	 629 606 None 621

INSTRUCTION	DESCRIPTION	FT
l n m TO 2	Gate nS signal to Uniservo (n) to alert Read and Forward thyratrons. Gate RP and FP signals to fire Read and Forward thyratrons in Uniservo (n). Gate RP to set Read Interlock. Gate LE of FT604 to ending pulse delay. If Direction Memory agrees with first instruction digit, supply Read Tape Preset and gate an EP to control circuits. Gate EP to set Read Forward and Start Read FF's after appropriate delay. * * Length of time before Read Forward FF is set is determined by condition of Reversal Memory. Length of time before Read Control FF is set is determined by condition of Reversal Memory and First Block Memory.	629 604 609 614

INSTRUCTION	DESCRIPTION	FT
2 n m	60 words from tape to rI, backward	
1	Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo desired will pass interlock.	629
	Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start read operation. + ≠	606
	If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At following t1 gate a pulse to generate IRP. *	None
	Gate IRP as Sequence I Preset.	621
	+ Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms.	
	* IRP is used to: 1. Step PC. 2. Set TO. 3. Supply reset pulse to Direction Memory. 4. Set Reversal Memory if FIR was returned from Uniservo. 5. Reset Interlock Release FF. 6. Supply Sequence I Preset.	
	≠ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.)	
TO		

INSTRUCTION	DESCRIPTION	FT
2 n m	Gate nS signal to Uniservo (n) to alert Read and Backward thyratrons.	629
2	Gate RP and BP signals to fire Read and Backward thyratrons in Uniservo (n). + Gate RP to set Read Interlock. Gate LE of FT604 to ending pulse delay.	604
	If Direction Memory agrees with First Instruction Digit, supply Read Tape Preset and gate an EP to control circuits.	609
	Gate EP to set Read Backward and Start Read FF's after appropriate delay. *	614
	* Length of time before Read Backward FF is set is determined by condition of Reversal Memory. Length of time before Read Control FF is set is determined by condition of Reversal Memory and First Block Memory.	
3 n m	(rI) ⟶ m THRU m+59; 60 words ⟶ rI, forward	
1	Operate rM address exceeded & preset checkers.	860
	Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo desired will pass interlock.	629
	Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start read operation. + ≠	606
	If FIR, BIR or FIR-BIR pass interlock test set Interlock Release FF. At following t1 generate IRP. *	None
	Gate IRP as Sequence I Preset.	621
	+ Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. IO-INT FF is reset. 4. First Block Memory is reset. 5. No rewind has been initiated within 3 ms.	
	* IRP is used to 1. Step PC. 2. Set TO. 3. Supply set pulse to Direction Memory. 4. Set Reversal Memory if BIR was returned from Uniservo. 5. Reset Interlock Release FF. 6. Supply Sequence I Preset.	
	≠ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.)	

INSTRUCTION	DESCRIPTION	FT
3 n m		
TO		
2	Set rM Read FF.	820
	Set BCM to RM.	827
	Inhibit set of M1 cores, strobe rI sense amplifiers, transfer $M_2 \rightarrow M_1$ and $M_2 \rightarrow rI$. Step rI address counters for each word transfer until "59" signal occurs, at which time set MTO, step PC, and set TO.	641
	Develop Serialize Pulse.	824
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Step rM and rZW address counters.	833
	Gate nS signal to Uniservo (n) to alert Read and Forward thyratrons.	629
	Gate RP and FP signals to fire Read and Forward thyratrons in Uniservo (n).	
	Gate RP to set Read Interlock. Gate LE of FT604 to ending pulse delay.	604
TO		
3	If Direction Memory agrees with First Instruction Digit, supply Read Tape Preset and gate an EP to control circuits.	609
	Gate EP to set Read Forward and Start Read FF's after appropriate delay. *	614
	* Length of time before Read Forward FF is set is determined by condition of Reversal Memory. Length of time before Read Control FF is set is determined by condition of Reversal Memory and First Block Memory.	

INSTRUCTION	DESCRIPTION	FT
4 n m	(rI) ⟶ m THRU m+59; 60 words ⟶ rI, backward	
1	Operate address exceeded & preset checkers.	860
	Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo desired will pass interlock.	621
	Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start read operation. + ≠	606
	If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At following t1 generate IRP. *	None
	Gate IRP as Sequence I Preset.	629
	+ Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms.	
	* IRP is used to: 1. Step PC. 2. Set TO. 3. Supply reset pulse to Direction Memory. 4. Set Reversal Memory if FIR was returned from Uniservo. 5. Reset Interlock Release FF. 6. Supply Sequence I Preset.	
	≠ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.)	
TO		
4 n m	Set rM Read FF.	820
	Set BCM to RM.	827
2	Inhibit set of M_1 cores, strobe rI sense amplifiers, transfer $M_2 \longrightarrow M_1$ and $M_2 \longrightarrow$ rI.	
	Step rI address counters for each word transferred until "59" signal occurs at which time set MTO, step PC, and set TO.	641
	Develop Serialize Pulse.	824
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Step rM and rZW address counters.	833
	Gate nS signal to Uniservo (n).	629
	Gate RP to set Read Interlock. Gate LE of FT604 to ending pulse delay.	604

INSTRUCTION	DESCRIPTION	FT
4 n m 3	If Direction Memory agrees with First Instruction Digit, supply Read Tape Preset and gate an EP to control circuits. Gate EP to set Read Backward and Start Read FF's after appropriate delay. * * Length of time before Read Backward FF is set is determined by conditions of Reversal Memory and First Block Memory.	 609 614
5 n m 1	(m THRU m+59)⟶tape, 215 pulses per inch. 108 pulses per inch if (n) Tape Density button is depressed. Operate rM address exceeded & preset checkers. Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo will pass interlock. Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start write operation. + ≠ % If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At the following t1 generate IRP. * Gate IRP to generate Sequence "0" Preset. + Computer will pass interlock if: 1. Write Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms. 6. Supervisory Control Interlock FF is reset. ≠ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set output of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.) % Gated F and W signal from the First Instruction Digit samples ring switch on Uniservo (n). If tape on Uniservo (n) is ringed, inhibit return of FIR, BIR or FIR-BIR. * IRP is used to: 1. Step PC. 2. Set TO. 3. Set Reversal Memory if BIR was returned from Uniservo. 4. Reset Interlock Release FF. 5. Supply Sequence "0" Preset.	 860 629 606 None 669

INSTRUCTION	DESCRIPTION	FT
5 n m	Sequence rM for RH timing.	820
	Strobe rM sense amplifiers.	821
TO	Transfer $M_1 \rightarrow M_3$.	829
	Transfer $M_3 \rightarrow r0$.	
2	Step r0 address counters for each word transferred until "59" signal occurs, at which time set MTO, step PC, and set TO.	681
	Step rM, rZW address counters.	833
	Develop Serialize Pulse	824
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Gate nS signal to Uniservo (n) and alert Write and Forward thyratrons.	629
	Gate WP and FP signals to fire Write and Forward thyratrons in Uniservo (n). Gate WP signal to set Write Interlock. Gate LE of FT604 to ending pulse delay. +	604
	+ If nS signal agrees with Tape Density Selector switch, gate WP to pick up Tape Density relay for 108 PPI.	
TO		
3	Supply Write Tape Preset and gate an EP to control circuits.	609
	Gate EP to set Write Forward and Start Write FF's after appropriate delay.*	615
	* Length of time before Write Forward FF is set is determined by condition of Reversal Memory. Length of time before Write Control FF is set is determined by condition of Reversal Memory and First Block Memory.	

INSTRUCTION	DESCRIPTION	FT
6 n m 1	Rewind Uniservo (n) Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo desired will pass interlock. Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start rewind operation. + ≠ If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At following t1 generate IRP. * Inhibit step PC, supply EP if Uniservo is rewound. + Computer will pass interlock if: 1. Write Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms. 6. Supervisory Control Interlock FF is reset. * IRP is used to: 1. Step PC. 2. Set TO. 3. Set Reversal Memory if FIR was returned from Uniservo. 4. Reset Interlock Release FF. ≠ If FIR-BIR is returned from Uniservo, set First Block Memory and inhibit IRP.	 629 606 None 608
TO		
2	Gate nS signal to alert Rewind and Backward thyratrons in Uniservo (n). Generate BP signal and supply pulse to initiate Rewind Start circuits, supply EP after Rewind Control FF is set.	629 619

INSTRUCTION	DESCRIPTION	FT
7 n m	(m THRU m+59) ⟶ tape; 54 pulses per inch	
1	Operate rM address exceeded & preset checkers.	860
	Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo desired will pass interlock.	629
	Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start write operation. + ≠ %	606
	If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF. At the following t1 generate IRP. *	None
	Gate IRP to generate Sequence "0" preset.	669
	+ Computer will pass interlock if: 1. Write Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms. 6. Supervisory Control Interlock FF is reset.	
	* IRP is used to: 1. Step PC. 2. Set TO. 3. Set Reversal Memory if BIR was returned from Uniservo. 4. Reset Interlock Release FF. 5. Supply Sequence "0" Preset.	
	≠ If FIR-BIR is returned from Uniservo, set First Block Memory gated by FIR-BIR and set of Interlock Release FF. (If First Block Memory is set, Reversal Memory will also be set.)	
	% Gated F and W signal from the First Instruction Digit samples ring switch on Uniservo (n). If tape on Uniservo (n) is ringed, inhibit return of FIR, BIR or FIR-BIR.	
TO		

INSTRUCTION	DESCRIPTION	FT
7 n m		
	Set rM Read FF, set M_1 cores.	820
2	Strobe rM sense amplifiers.	821
	Transfer $M_1 \rightarrow M_3$.	829
	Step rM, rZW address counters.	833
	Transfer $M_3 \rightarrow$ r0. Step r0 address counters for each word transferred until "59" signal occurs at which time set MT0, step PC, and set T0.	681
	Develop Serialize Pulse.	824
	Operate HSB-0EC.	429
	Operate HSB-A0C.	428
	Set 54 pulses per inch thyratron to write at 54 PPI.	None
	Gate nS signal to Uniservo (n) to alert Write and Forward thyratrons.	629
	Gate WP and FP signals to fire Write and Forward thyratrons in Uniservo (n). Gate WP signal to set Write Interlock. Gate LE of FT604 to ending pulse delay.	604
T0		
3	Gate an EP to control circuits.	609
	Gate an EP to set Write Forward and Start Write FF's after appropriate delay.	615

INSTRUCTION	DESCRIPTION	FT
8 n m 1	Rewind Uniservo (n) with interlock Gate nS (Servo Selector) signal from Second Instruction Digit to determine if Uniservo desired will pass interlock. Gate FIR, BIR or FIR-BIR to determine if computer will pass interlock to start rewind operation. + ≠ If FIR, BIR or FIR-BIR passes interlock test, set Interlock Release FF (IRG), and at following t1 generate IRP. Gate IRG to pick Interlock relay in Uniservo (n). Inhibit step PC, supply EP if Uniservo is rewound. + Computer will pass interlock if: 1. Write Interlock is reset. 2. Reversal Memory is reset. 3. First Block Memory is reset. 4. IO-INT FF is reset. 5. No rewind has been initiated within 3 ms. 6. Supervisory Control Interlock FF is reset. ≠ If FIR-BIR is returned from Uniservo, set First Block Memory and inhibit IRP. NOTE: Uniservo will assume First Block condition if both Forward and Backward thyratrons are extinguished in the Uniservo.	 629 606 None 607 608
TO		
8 n m 2	Gate nS signal to alert Rewind and Backward thyratrons in Uniservo (n). Generate BP signal and supply pulse to initiate rewind start circuits. Supply EP after Rewind With Interlock relay is picked up and Rewind Control FF is set.	 629 619 607

INSTRUCTION	DESCRIPTION	FT
10 m	Supervisory keyboard ⟶ rM	
1	Operate rM address exceeded & preset checkers. Generate signal to pass Supervisory Control interlock provided that no Read, Supervisory Control Type-out, or Supervisory Control Type-in is in progress. Set Supervisory Control Input FF. Set Interlock Release FF provided that Reversal Memory, and First Block Memory is reset, and no rewind has been initiated within 3 ms. Gate following t1 as IRP. * Gate IRP as Sequence I Preset. * IRP is used to: 1. Step PC. 2. Set TO. 3. Reset Interlock Release FF. 4. Set Supervisory Control Input FF. 5. Supply Sequence I Preset.	860 616 None 621
TO		
2	The Sequence I Preset clears and presets the input counters. The K signals (result of setting Supervisory Control Input FF) control the Input Distributor Control circuits to facilitate a Supervisory Control input. Type in 6 digits, digit by digit, checking each digit for any odd-even error, and step TRI counters after each key is depressed. Transfer each digit from the N_5 cores to M_2. After the 6th digit is typed, transfer $M_2 \longrightarrow M_1$ and type in 6 more digits to M_2. After the 12th digit is typed, set Stop FF and depress Word Release which will step PC and set TO.	No FT
TO		
3	Set rM Read FF. Transfer $M_2 \longrightarrow M_1$, inhibit set of M_1 cores. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Set MTO. Supply EP.	820 645 824 429 428 825 206

INSTRUCTION	DESCRIPTION	FT
30 m	(rI) ⟶ m thru m+59	
1	Operate rM address exceeded & preset checkers.	860
	Generate "0 Select" signal from Second Instruction digit.	629
	Gate "0 Select" signal to determine if computer will pass interlock, to start transfer operation. +	606
	If "0 Select" passes interlock test, set Interlock Release FF. At following t1 gate a pulse to generate IRP. *	
	Gate IRP as Sequence I Preset.	621
	+ Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. IO-INT FF is reset. 4. First Block Memory is reset. 5. No rewind has been initiated within 3 ms.	
	* IRP is used to: 1. Step PC. 2. Set TO. 3. Supply set pulse to Direction Memory. 4. Reset Interlock Release FF. 5. Supply Sequence I Preset.	
TO		
2	Set rM Read FF	820
	Set BCM to RM.	827
	Strobe rI sense amplifiers transferring $M_2 \longrightarrow M_1$ and $M_2 \longrightarrow$ rI. Step rI address counters for each word transferred until "59" signal occurs, at which time set MTO, step PC, and set TO.	641
	Develop Serialize Pulse	824
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Step rM and rZW address counters.	833
		629*
	Gate LE of FT604 to ending pulse delay.	604
	* FT629 is brought up for a 30 instruction, but is not used because no Uniservo is operated.	
TO		
3	If Direction Memory agrees with instruction Gate EP to control circuits.	609
		614*
	* FT614 is brought up for a 30 instruction, but is not used because no Uniservo is operated.	

INSTRUCTION	DESCRIPTION	FT
40 m	(rI) ⟶ m thru m+59	
1	Operate rM address exceeded & preset checkers. Generate "0 Select" signal from Second Instruction Digit. Gate "0 Select" signal to determine if computer will pass interlock to start transfer operation. + If "0 Select" passes interlock test, set Interlock Release FF. At following t1 gate a pulse to generate IRP. * Gate IRP as Sequence I Preset.	860 629 606 621
	+ Computer will pass interlock if: 1. Read Interlock is reset. 2. Reversal Memory is reset. 3. IO-INT FF is reset. 4. First Block Memory is reset. 5. No rewind has been initiated within 3 ms. * IRP is used to: 1. Step PC. 2. Set TO. 3. Supply reset pulse to Direction Memory. 4. Reset Interlock Release FF. 5. Supply Sequence I Preset.	
TO		
2	Set rM read FF, set M_1 cores. Set BCM to RM. Inhibit set of M1 cores, strobe rI sense amplifiers transferring $M_2 \rightarrow M_1$ and $M_2 \rightarrow$ rI. Step rI address counters for each word transferred until "59" signal occurs at which time set MTO, step PC, and set TO. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Step rM and rZW address counters. Gate RP to set Read Interlock. Gate LE of FT604 to ending pulse delay. * FT629 is brought up for a 40 instruction, but is not used because no Uniservo is operated.	820 827 641 824 429 428 833 604 629*
TO		
3	If Direction Memory agrees with first instruction, gate an EP to control circuits. * FT614 is brought up for a 40 instruction, but is not used because no Uniservo is operated.	609 614*

INSTRUCTION	DESCRIPTION	FT
50	(Register determined by SC output button) → SC printer	
1	Operate rM address exceeded & preset checkers.	860
	Generate signal to pass Write Interlock at Write Interlock gate provided the Supervisory Control Interlock FF and Write Interlock FF are reset.	606
	Set Interlock Release FF provided the First Block Memory, Reversal Memory, IO-INT are reset, and no rewind has been initiated within 3 ms.	None
	Gate output of Interlock Release FF with a t1 to generate IRP. *	None
	Gate IRP to generate Sequence 0 Preset.	669
	Gate IRP to set Supervisory Control Output FF, set Write Interlock.	617 629+
	* IRP is used to: 1. Step PC. 2. Set TO. 3. Reset Interlock Release FF. 4. Set Supervisory Control Output FF. 5. Supply Sequence 0 Preset.	
	+ FT629 is picked up for a 50 instruction, but is used only in the FTOC.	

INSTRUCTION	DESCRIPTION	FT
50 TO 2	The Sequence 0 Preset clears and presets the output counters. The T signals (result of setting the Supervisory Control Output FF) control the Output Distributor control circuits to facilitate a Supervisory Control output.	
	Set rZW Read FF.	818
	Set rM Read FF, set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set MTO.	825
	Step PC, set TO.	214
	Above steps are for readout of rM. With FT 820, 821, and 824 deleted, and FT 823, 826, 861 and the read out FT of a particular register inserted, a register type out is accomplished. The sequence for type out from a register is:	
	Set rZW Read and Write FF's	818*
	Transfer (rA) ⟶ HSB.	100+
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Develop Staticize Pulse	823
	Set MTO.	825
	Step PC, set TO.	214
	Set rZW Read FF, set M_1 cores.	826
	Inhibit set of rM Read/Write FF.	861
	+ Up only if rA Output Selector button is depressed.	
	Other FT signals are:	
	1. rF 192	
	2. rL 187	
	3. rA 100	
	4. rX 125	
	5. CC 210	
	6. CR 248	
	* The EP gated by FT818 in the Control Circuits is suppressed by FT214.	
TO		

INSTRUCTION	DESCRIPTION	FT
50	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
3	Set rZW Read/Write FF's.	818
	Strobe rZW sense amplifiers.	819
	Set rZW Read FF, set M_1 cores.	820
	Develop Serialize Pulse.	824
	Set MTO.	825
	Transfer $M_1 \longrightarrow M_3$.	829
	Inhibit set of rM Write FF.	861
	Transfer $M_3 \longrightarrow M_4$.	685
	Step PC, set TO.	214
TO		
4	Supply EP.	206
50 Breakpoint	(Register determined by SC output button) $\longrightarrow$ SC printer	
	Stop computer if Type Out Breakpoint switch on SC is operated.	
1	Operate rM address exceeded & preset checkers.	860
	Generate signal to pass write interlock at Write Interlock gate provided that Supervisory Control Interlock FF and Write Interlock FF is reset.	606
	Set Interlock Release FF provided that, First Block Memory, Reversal Memory, IO-INT are reset, and no rewind has been initiated within 3 ms.	None
	Gate output of Interlock Release FF with a t1 to generate IRP. *	None
	Gate IRP to generate Sequence 0 Preset.	669
	Gate IRP to set Supervisory Control Output FF, set Write Interlock.	617
	Set Stop FF if Output Breakpoint switch is thrown.	218
		629+
	* IRP is used to: 1. Step PC 2. Set TO 3. Reset Interlock Release FF 4. Set Supervisory Control Output FF 5. Supply Sequence 0 Preset	
	+ FT 629 is picked up for a 50 instruction, but is used only in the FTOC.	

INSTRUCTION	DESCRIPTION	FT
TO 50 Breakpoint 2	The Sequence 0 Preset clears and present the output counters. The T signals (result of setting the Supervisory Control Output FF) control the Output Distributor control circuits to facilitate a Supervisory Control output.	
	Set rZW Read FF.	818
	Set rM Read FF, set M1 Cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set MTO.	825
	Step PC, set TO.	214
	Above steps are for read out of rM. With FT 820, 821, and 824 deleted and FT 823, 826, 861, and the read out FT of a particular register inserted, a register type out is accomplished. The sequence for read out from a register is:	
	Transfer (rA) ⟶ HSB.	100+
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Develop Staticize Pulse.	823
	Set MTO.	825
	Step PC, set TO.	214
	Set rZW Read FF.	826
	Inhibit set of rM Read/Write FF's.	861
	Set rZW Read FF.	818*
	+ Up only if rA Output Selector button is depressed.	
	Other FT signals are:	
	1. rF 192	
	2. rL 187	
	3. rA 100	
	4. rX 125	
	5. CC 210	
	6. CR 248	
	*The EP gated by FT818 in the control circuits is suppressed by FT214.	
TO		

INSTRUCTION	DESCRIPTION	FT
50 Breakpoint		
3	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rZW Read/Write FF's.	818
	Strobe rZW sense amplifiers.	819
	Set rZW Read FF, Set M_1 Cores.	820
	Develop Serialize Pulse.	824
	Set MTO.	825
	Transfer $M_1 \rightarrow M_3$.	829
	Inhibit rM Write FF.	861
	Transfer $M_3 \rightarrow M_4$.	685
	Step PC, set TO.	214
TO		
4	Supply EP.	206
50 Skip	(Register determined by SC output button) $\rightarrow$ Printer.	
	Skip the type out if Skip Type Out switch on SC is operated.	
	Supply EP (if switch is operated)	206
Empty	rM, successive words $\rightarrow$ SC printer	
1	Operate rM address exceeded & preset checkers.	860
	Insert decimal zeros onto HSB.	401
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Operate HSB $\rightarrow$ CR gate, operate CR clear gate.	201
	Generate a signal to pass write interlock at Write Interlock gate provided the Supervisory Control Interlock FF and Write Interlock are reset.	606
	Set Interlock Release FF provided the First Block Memory, Reversal Memory, IO-INT are reset and no rewind has been initiated within 3 ms.	None
	Gate output of Interlock Release FF with a t1 to generate IRP.	None
	Gate IRP to generate Sequence 0 Preset.	669
	Gate IRP to set Supervisory Control Output FF, to Write Interlock.	617
		629+
	* IRP is used to: 1. Step PC. 2. Set TO. 3. Reset Interlock Release FF. 4. Set Supervisory Control Output FF. 5. Supply Sequence 0 Preset.	
	+FT629 is picked up for an EMPTY instruction, but is used only in FTOC.	
TO		

INSTRUCTION	DESCRIPTION	FT
2	The Sequence 0 Preset clears and presets the output counters. The T signals (result of setting the Supervisory Control Output FF) control the Output Distributor control circuits to facilitate a Supervisory Control output.	
	Set rM Read FF, Set M_1 cores.	820
	Strobe rM sense amplifiers.	821
	Develop Serialize Pulse.	824
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set MTO.	825
	Step PC, set TO.	214
TO		
Empty 3	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Set rZW Read/Write FF's.	818
	Set rM Read FF, Set M_1 Cores.	820
	Strobe rZW sense amplifiers	819
	Develop Serialize Pulse.	824
	Set MTO.	825
	Transfer $M_1 \longrightarrow M_3$.	829
	Inhibit set of rM Read/Write FF's.	861
	Read M_3, transfer $M_3 \longrightarrow M_4$.	685
	Step PC, set TO.	214
Empty TO		
4	Transfer CC $\longrightarrow$ min input adder, (000000 000001) sub input adder. Transfer sum from unbarred adder to CC after clearing CC.	212
	Operate adder for 12-place addition.	714
	Operate adder OE and sum comparison checkers.	435
	Supply reset pulse to Overflow FF.	737
	Transfer (CR) $\longrightarrow$ SR distributor line without delay.	204
	Supply EP.	206
	Note: EMPTY instruction is started by depressing the Empty switch on SC. It is executed in Beta time with the typed information being read from rM location, designated by SR - the current CC reading. After the EP, two skip instructions will be executed because of the decimal zeros read into CR during PG-1, thus permitting (CC) to set up into SR with next memory to be emptied.	

INSTRUCTION	DESCRIPTION	FT
Fill	SC keyboard → rM, successive words	
1	Operate rM address exceeded & preset checkers.	860
	Insert decimal zeros onto HSB.	401
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Operate HSB → CR gate, Operate CR clear gate	201
	Generate signal to pass Supervisory Control Interlock, provided that no read, Supervisory Control type-out, or Supervisory Control type-in is in progress.	616
	Set Interlock Release FF, provided that Reversal Memory and First Block Memory are reset, and no rewind has been initiated within 3 ms. Gate following t1 as IRP. *	None
	Gate IRP as Sequence I Preset.	621
	* IRP is used to: 1. Step PC. 2. Set TO. 3. Reset Interlock Release FF. 4. Set Supervisory Control Input FF. 5. Supply Sequence I Preset.	
Fill TO		
2	The Sequence I Preset clears and presets the input counters. The K signals (result of setting Supervisory Control Input FF) control the Input Distributor control circuits to facilitate a Supervisory Control input. Type in 6 digits, digit by digit, check each digit for an odd-even error, and step TRI counters after each key is depressed. Transfer each digit from the N_5 cores to M_2. After the 6th digit is typed, transfer $M_2 \rightarrow M_1$ and type in 6 more digits to M_2. After the 12th digit is typed, set Stop FF and depress Word Release which will step PC and set TO.	No FT
TO		

INSTRUCTION	DESCRIPTION	FT
3	Set rM Read FF, set M_1 Cores.	820
	Read M_2. Transfer $M_2 \longrightarrow M_1$.	645
	Develop Serialize Pulse.	824
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Transfer CC $\longrightarrow$ min input adder, (000000 000001) to sub input adder. Transfer sum from unbarred adder to CC after clearing CC.	212
	Operate adder for 12-place addition.	714
	Operate adder OE and sum comparison checkers.	435
	Supply reset pulse to Overflow FF.	737
	Transfer (CR) $\longrightarrow$ SR Distributor Line without delay.	204
	Set MTO.	825
	Supply EP.	206
	Note: FILL instruction is started by moving the CR Interlock/Fill Mem switch on Supervisory Control to the Fill Mem position. It is executed in Beta time with the typed information going to the memory location designated by the SR, which contains the current CC reading. After the EP two skip instructions will be executed because of the decimal zeros read into CR during PC-1, thus permitting (CC) to set up in SR the next memory address to be filled.	
Clear CC	CU (000000 000000) $\longrightarrow$ CC	
	Connect CU (000000 000000) to HSB.	401
	Operate HSB-OEC.	429
	Operate HSB-AOC.	428
	Connect HSB to CC, clear CC.	208
	Supply EP.	206
	Note: By depressing the clear C switch on Supervisory Control, CY is automatically jammed to Beta, and the addition of one to (CC) is inhibited.	

INSTRUCTION	DESCRIPTION	FT
SCI-CR	One word S C keyboard ⟶ CR	
1	Generate signal to pass Supervisory Control interlock provided that no read, Supervisory Control type-out, or Supervisory Control type-in is in progress.	616
	Set Interlock Release FF provided that Reversal Memory, First Block Memory, and Rewind Frequency control is reset. Gate t1 after setting Interlock Release FF as IRP. *	None
	Gate IRP as Sequence I Preset.	621
	Gate IRP to set Supervisory Control FF.	616
	Supply reset pulse to Overflow FF.	737
	* IRP is used to: 1. Step PC. 2. Set TO. 3. Reset Interlock Release FF. 4. Set Supervisory Control FF. 5. Supply Sequence I Preset.	
TO		
2	The Sequence I Preset clears and presets the input counters. The K signals (result of setting Supervisory Control Input FF) control the Input Distributor control circuits to facilitate a Supervisory Control input. Type in 6 digits, digit by digit, check each digit for an odd-even error, and step TRI counters after each key is depressed. Transfer each digit from the N_5 cores to M_2. After the 6th digit is typed, transfer $M_2 \longrightarrow M_1$ and type in 6 more digits to M_2. After the 12th digit is typed, set Stop FF, depress Word Release which will step PC and set TO.	No FT
TO		
3	Inhibit set of rM Read/Write FF's.	861
	Enable set of rZW Read FF.	818
	Develop Serialize Pulse.	824
	Set rZW Read FF, set M_1 Cores	820
	Read M_2, transfer $M_2 \longrightarrow M_1$.	645
	Set MTO.	825
	Operate HSB-OEC	429
	Operate HSB-AOC	428
	Step PC, set TO, and inhibit EP supplied by FT818.	214

INSTRUCTION	DESCRIPTION	FT
SCI-CR 4	Preset BCM to RM. Inhibit rM Read/Write FF. Enable set of rZW Read/Write FF's. Set rZW Read FF. Strobe rZW sense amplifiers. Develop Serialize Pulse. Operate HSB-OEC. Operate HSB-AOC. Connect HSB to CR, clear CR. Read LH(CR)→SR. Set MTO. Supply EP NOTE: CR TYPE IN switch will jam CY to Beta, and set up SR for SCI-CR.	827 861 818 820 819 824 429 428 201 204 825 206
Memory Clear	Connect CU (000000 000000) to HSB. Operate HSB-OEC. Operate HSB-AOC. Develop Staticize Pulse. Set rM Read FF, set M_1 Cores. Operate rM address exceeded and preset checkers. Set MTO.	401 429 428 823 826 860 825

4. CONDENSED INSTRUCTION REFERENCE.

This section is similar to Section 3 in that it lists the instructions, in order and by PC steps. However, it lists the FT signals associated with each PC step by number only, and not with description. This offers a rapid reviewal of FT signals present during maintenance routines.

Instruction	Program Counter Step	FT Signals	Notes
A	1	120, 126, 214, 429, 820, 821 824, 825, 827, 428, 860	In all cases a PC step not shown for an F order is the same as that step without "F".
	2	109, 125, 160, 206, 435	
AF	1	120, 126, 193, 214, 429, 820 821, 824, 825, 827, 428, 860	
AH	1	Same as A PC 1	
	2	Same as A PC 2, inhibit 206, pick up 214	
	3	Same as H	
B		101, 105, 120, 126, 206, 429, 820, 821, 824, 825, 827, 428, 860	
BF		101, 105, 120, 126, 193, 206, 429, 820, 821, 824, 825, 827, 428, 860	
C		100, 206, 429, 823, 825, 826, 860, 428, 101, 108	
D	1	101, 105, 138, 151, 152, 214, 429, 820, 821, 824, 825, 827, 860, 428	
	2	101, 103, 159, 171, 214, 226	
D	3-14	109, 145, 159, 188, 246, 435, 714	
	14	228, 244	
	15	101, 109, 111, 125, 159, 214 435, 714	
	16	101, 106, 120, 123, 159, 161, 206	
DF	1	101, 105, 138, 151, 152, 193 214, 429, 820, 821, 824, 825 827, 428, 860	
E		193, 206, 429, 820, 821, 824, 825, 827, 832, 428, 860, 101, 105	

EF	1	193, 214, 429, 820, 821, 824, 101 825, 827, 831, 832, 860, 428, 105
	2	100, 206, 429, 823, 825, 826 860, 428
F		190, 206, 429, 820, 821, 824 825, 827, 860, 428
G		192, 206, 429, 823, 825, 826 860, 428
H		100, 206, 429, 823, 825, 826, 860, 428
I		187, 206, 429, 823, 825, 826, 860, 428
J		125, 206, 429, 823, 825, 826, 860, 428
K		100, 101, 108, 185, 206, 429, 428
L		120, 126, 185, 206, 429, 820, 821, 824, 825, 827, 860, 428
LF		120, 126, 185, 193, 206, 429, 820, 821, 824, 825, 827, 428, 860
MP	1	101, 108, 110, 113, 120, 126, 139, 214, 429, 435, 820, 821, 824, 825, 827, 860, 428
MNP	2	110, 113, 214, 435, 714
MNP	3	110, 113, 151, 214, 435, 714
MN	4	100, 101, 108, 112, 113, 120, 123, 159, 190, 214, 226, 435, 428, 429
NMP	5-15	109, 147, 159, 188, 246, 435, 714
MNP	14	244
MNP	15	149, 161, 215, 228

MF-PF	1	101, 108, 110, 113, 120, 126, 139, 193, 214, 429, 435, 820, 821, 824, 825, 827, 860, 428	
*N	1	101, 108, 110, 113, 120, 139 153, 214, 429, 435, 820, 821, 824, 825, 827, 860, 428	*(N, NFP and PF have P C steps and same FT signals as M and MF except as noted)
*Nf	1	101, 108, 110, 113, 120, 139, 153, 193, 214, 429, 435, 820, 821, 824, 825, 827, 860, 428	
*P	4	100, 101, 108, 112, 120, 123, 159, 190, 214, 226, 429, 428	**If 2nd Inst. digit is zero treat Instruction as skip if compatibility switch is set to Univac II.
Q	1	152, 156, 187, 214, 236, 429, 428	
	2	159, 200, 206, 209, 429, 428	
R		206, 245, 429, 823, 825, 826 860, 428	
S	1	120, 153, 214, 429, 820, 821, 824, 825, 827, 860, 428	
	2	109, 125, 160, 206, 435	
SF	1	120, 153, 193, 214, 429, 820, 821, 824, 825, 827, 860, 428	
SH	1	Same as S PC 1	
	2	109, 125, 160, 214, 435	
	3	100, 206, 429, 823, 825, 826, 860, 428	
T	1	152, 172, 187, 214, 236, 429, 428	
	2	159, 200, 206, 209, 429, 428	
U		200, 206, 208, 429, 428	
V		429, 817, 818, 820, 821, 824, 827, 833, 860, 428, 206**	

ANALYSIS OF INSTRUCTIONS		UNIVAC II
W		429, 817, 818, 819, 820, 824, 827, 833, 860, 428, 206**
X		109, 125, 160, 206, 400, 435
Y		429, 816, 818, 820, 821, 824, 827, 833, 860, 428, 206*
Z		428, 429, 816, 818, 819, 820 824, 827, 833, 860, 206*
.n all		101, 106, 213, 817, 818, 833
-n all		107, 170, 213, 817, 818, 833
;n all		101, 103, 171, 213, 817, 818, 833
0 n all		104, 170, 171, 213, 817, 818, 833.
00		206
.0		206, 217
90		206, 218
1n	1	606, 621, 629
	2	609, 604, 614, 629
2n	1	606, 621, 629
	2	609, 604, 614, 629
3n	1	606, 621, 629, 860,
	2	429, 604, 629, 641, 820, 824, 827, 833, 428
	3	609, 614
4n	1	606, 621, 629, 860,
	2	429, 604, 629, 641, 820, 824, 827, 833, 428
	3	609, 614
5n	1	606, 629, 669, 860

*If 2nd Inst. digit is a 7, 8, 9 or 0 and if compatibility switch is set to Univac II treat instruction as skip.

** If 2nd Inst. digit is zero and compatibility switch is set to Univac II, treat instruction as a Skip.

5n	2	429, 604, 629, 681, 820, 821, 824, 829, 833, 428
	3	609, 615
6n	1	606, 608, 629
	2	619, 629
7n	1	606, 629, 669, 860
	2	429, 604, 629, 681, 820, 821, 824, 829, 833, 428
	3	609, 615
8n	1	606, 607, 608, 629
	2	607, 619, 629
10m	1	616, 621, 860
	2	
	3	206, 428, 429, 645, 820, 824, 825
10, CR	1	616, 621, 737,
	2	
	3	645, 818, 820, 825, 861, 214, 428, 429, 824
	4	201, 203, 428, 429, 818, 819, 820, 824, 825, 827, 861, 206
30		Same as 3n except 0 Selector signal prevents tape operation.
40		Same as 4n except 0 Selector signal prevents tape operation.
50	1	606, 617, 669, 629*, 860
	2	214, 429, 685, 825, 818, 428
		M 820, 821, 824
		A 100, 823, 826, 861
		X 125, 823, 826, 861

*Note 629 is picked up but used only in FTOC.

50	2	L	187, 823, 826, 861
		F	192, 823, 826, 861
		CC	210, 823, 826, 861
		CR	248, 823, 826, 861
	3		214, 428, 429, 685, 818, 819, 820, 824, 825, 861, 829
	4		206
50 Breakpoint			
	1		218, 606, 617, 669, 629, 860
	2		Same as 50 PC-2
	3		Same as 50 PC-3
	4		Same as 50 PC-4
50 Skip	1		206
*Fill	1		201, 401, 428, 429, 616, 621,
	2		
	3		206, 429, 645, 820, 824, 825
*Empty	1		201, 401, 429, 606, 617, 669, 860, 428
	2		214, 429, 820, 821, 824, 825, 428, 818
	3		214, 428, 429, 685, 818, 819, 820, 824, 825, 829, 861
	4		206
Clear CC			206, 208, 401, 428, 429
β Compute			201, 206, 429, 820, 821, 824, 825, 827, 860, 428
BETA			204, 212, 435, 714, 737
GAMMA			203, 203K
DELTA			850, 203K
Memory Clear			401, 429, 823, 826, 860, 428, 825

*Beta cycle is allowed to excite on PC4 of Fill or PC3 of Empty. (F.T. 204, 212, 435, 714, 737 are up during Beta)

5. DESCRIPTION OF FUNCTION TABLE SIGNALS.

The Function Table signals described on the following pages generate the minor sequences which complete the instruction routines. The FT signals are initiated by either the decoding of a programmed instruction or by some element of the automatic interval programming of the computer. Figure 1 presents, logically, the signals which control the alerting of the FT signals.

The FT signals are listed in the numerical order of their assigned numbers. Duplicated signals are indicated with the barred notation, e.g., 100 and $\overline{100}$. In the instances where an FT signal originates from several drivers, symbols are used following the FT signal number to differentiate between the various outputs to facilitate identification in the outlying circuits, e.g. FT160A, FT160B, FT160C, etc. Most FT signals are negative-going, those that are not usually carry a plus sign following the FT number; e.g. FT645+.

Pertinent information concerning the FT signals is presented in the columns following the FT number. Column 1 locates the chassis in which the FT signal is generated and gives the output terminal on which the FT signal appears. Column 2 lists the test terminal, for maintenance purposes, on which the full signal appears. Column 3 names the vacuum tube on the chassis from which the FT signal appears. Column 4 lists the signal-no signal condition of the FT signal; i.e., the voltage levels that appear on the corresponding test terminal of the FT. Column 5 provides a logical description of the function performed by each FT signal.

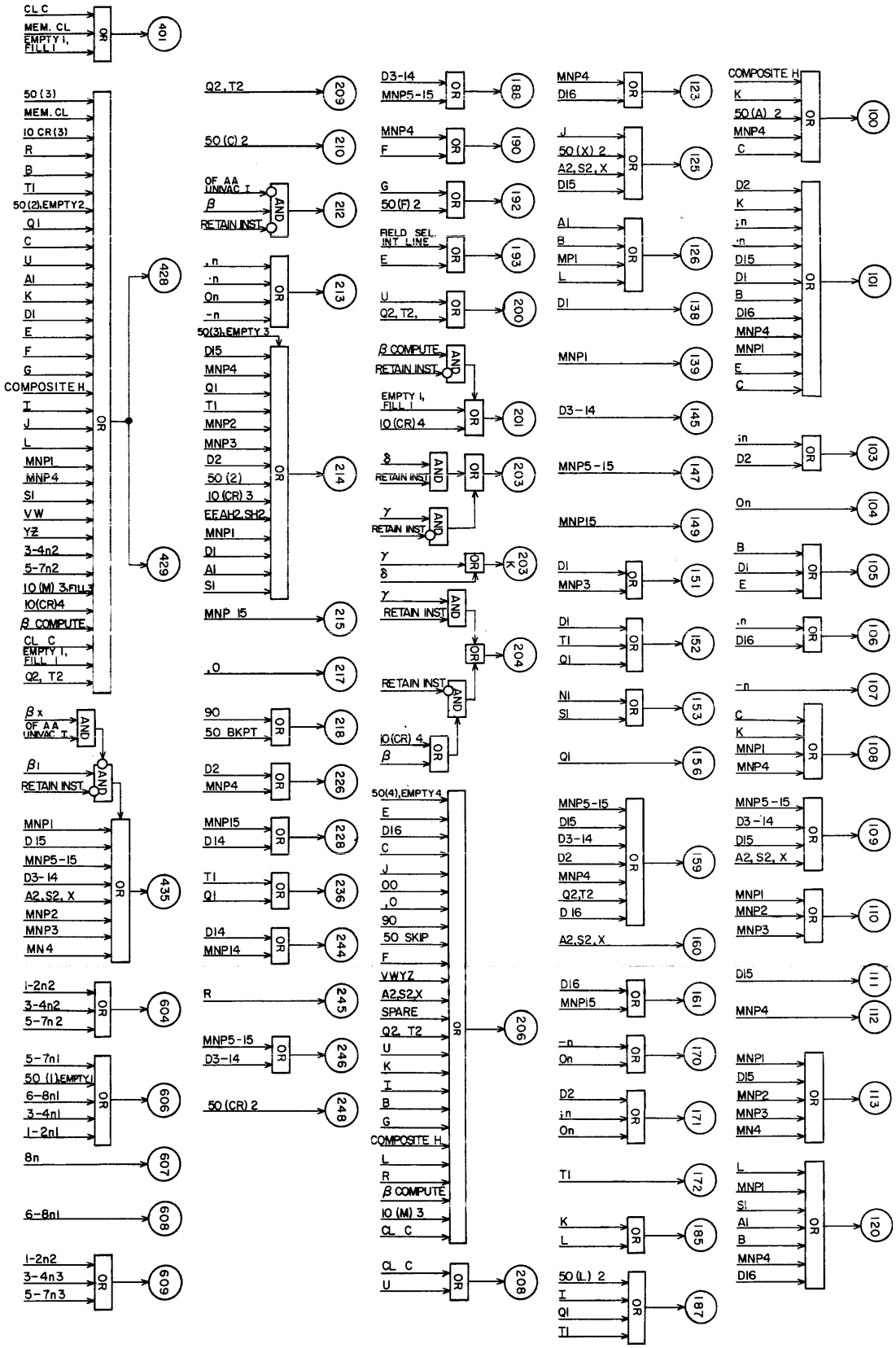

Figure 1. Logical Diagram, Function Table Signals

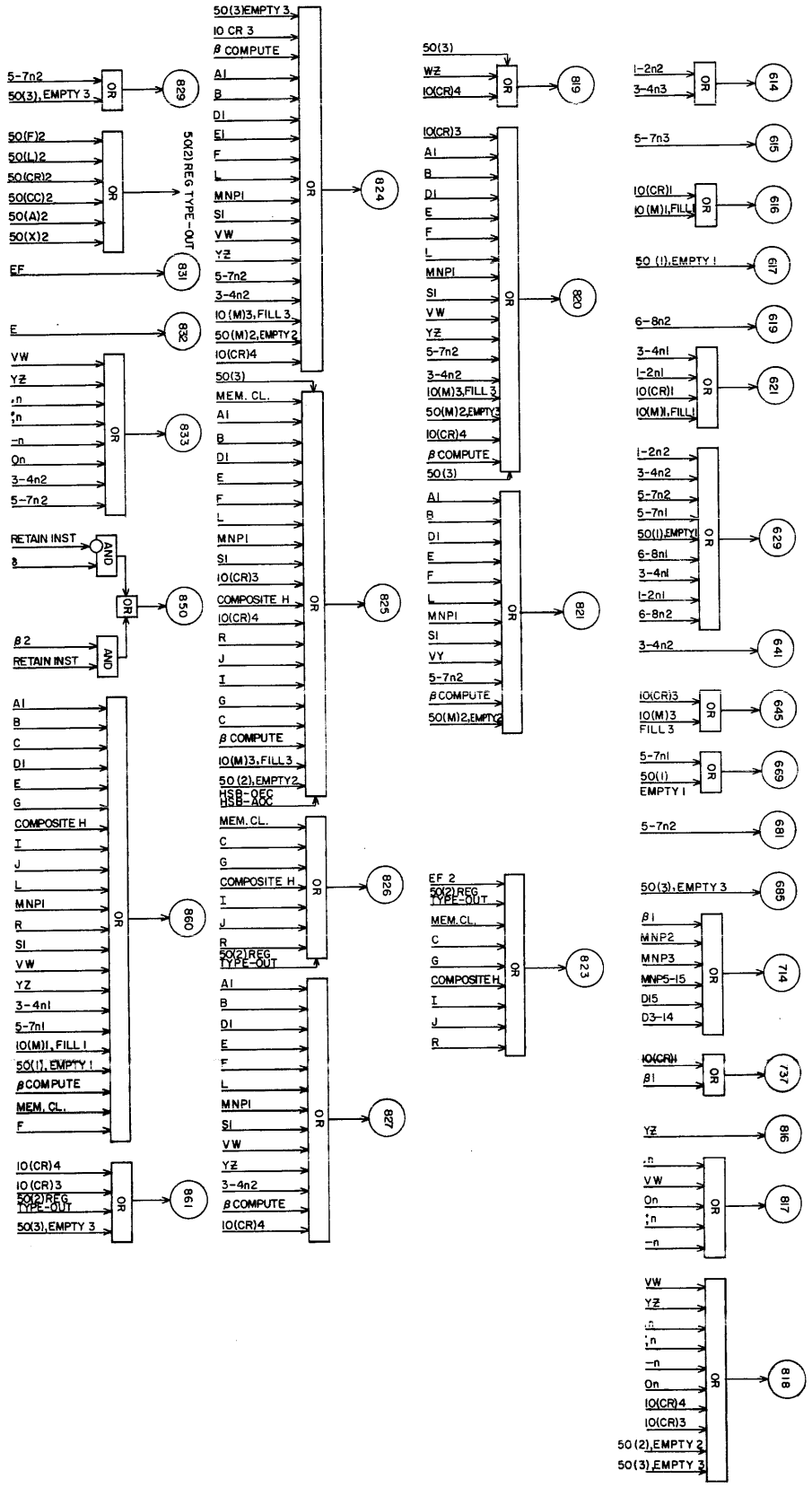

Figure 1. Logical Diagram, Function Table Signals (cont'd.)

Function Table	Chassis	TT	Tube	S/NS	Definition
100	B5T28	A2	V1	60/90	Connect rA to HSB.
$\overline{100}$	B5T29	A4	V2	60/90	
101	B3T65	C2	V5	60/90	Operate rA clear gate.
$\overline{101}$	B3T33	C1	V4	60/90	
103	B10T54	A12	V1	60/90	Operate left shift path of rA (including sign).**
$\overline{103}$	B10T29	A13	V2	60/90	
104	B10T85	G6	V13	60/90	Operate left shift path of rA (excluding sign).**
$\overline{104}$	B10T87	G7	V14	60/90	
105	B3T43	E4	V8	60/90	Connect HSB to rA.
$\overline{105}$	B3T38	C7	V7	60/90	
106A	B12T56	A4	V2	60/90	Operate right shift path of rA.
$\overline{106A}$	B12T54	A2	V1	60/90	
106B	B12T62	A7	V4	60/90	Insert decimal zero into sign position in rA.
$\overline{106B}$	B12T60	A6	V3	60/90	
106C	B12T39	C4	V6	60/90	Transfer sign from comparator to rA and rX.
$\overline{106C}$	B12T35	C3	V5	60/90	
107	B10T46	G1	V11	60/90	Operate right shift path of rA, and insert a decimal zero into the MSD position.*
$\overline{107}$	B10T81	G3	V12	60/90	
108	C1V66	C6	V6	60/90	Connect CU (000000 000000) to rA.
$\overline{108}$	C1V33	C3	V5	60/90	
109A	C4V60	A6	V3	60/90	Connect HSB to adder sub input.
$\overline{109A}$	C4V62	C1	V4	60/90	

** rA shifts one digit left for each minor cycle of Time-On.

* rA shifts one digit right for each minor cycle of Time-On.

Function Table	Chassis	TT	Tube	S/NS	Definition
109D	C4V66	C4	V5	60/90	Connect rA to adder min input. Clear rA and transfer sum from adder to rA.
$\overline{109D}$	C4V68	C6	V6	60/90	
110	~~C3B56~~ C3V56	A2	V1	60/90	Connect rL to adder sub input. Transfer (rL) to adder, replacing sign digit with a decimal zero.
$\overline{110}$	C3V29	A4	V2	60/90	
111	B5T85	G5	V13	60/90	Connect CU (round-off 000000 000005) to adder min input.
$\overline{111}$	B5T87	G7	V14	60/90	
112A	B11T70	C7	V7	60/90	Connect CU (050000 000000) to the adder sub input.
$\overline{112A}$	B11T73	E3	V8	60/90	
112B	B11T75	E6	V9	60/90	Clear MQC to binary zero and set up nines complement of digit in MQC.
$\overline{112B}$	B11T77	E8	V10	60/90	
112C	B11T81	G2	V11	60/90	Transfer the LSD of (rX) to MQC.
$\overline{112C}$	B11T83	G4	V12	60/90	
113	B3T87	G7	V14	60/90	Connect rA to adder min input. Clear rA and read sum from adder to rA (transfer ends at t12 to T0).
$\overline{113}$	B3T83	G6	V13	60/90	
120	B3T31	A7	V3	60/90	Operate rX clear gate.
$\overline{120}$	B3T58	A6	V2	60/90	
123	C1V62	A8	V4	60/90	Operate right shift path in rX.
$\overline{123}$	C1V31	A7	V3	60/90	
125	B5T67	C6	V6	60/90	Connect rX to HSB.
$\overline{125}$	B5T72	C8	V7	60/90	
126	C1V73	E3	V8	60/90	Connect HSB to rX.
$\overline{126}$	C1V70	C6	V7	60/90	
138A	B8T60	A7	V3	60/90	Clear MQC to decimal zero.
$\overline{138A}$	B8T64	A8	V4	60/90	

Function Table	Chassis	TT	Tube	S/NS	Definition
138B	B8T66	C3	V5	60/90	Preset BC-120 in MQC to the non-complement state thereby alerting the non-complementing gates between MQC and MQC-FT.
$\overline{138B}$	B8T68	C6	V6	60/90	
139	B8T71	E2	V7	60/90	Preset BC-120 to the complement state, thereby alerting the complement gates connecting the MQC and MQC-FT.
$\overline{139}$	B8T73	E3	V8	60/90	
145A	C5V62	C1	V4	60/90	Gate non-complement output of BC-120 to operate Improper Division Detector in MQC.#
$\overline{145A}$	C5V60	A6	V3	60/90	
145B	C5V68	C6	V6	60/90	Enable non-complement output of BC-120 to develop SIX signal.
$\overline{145B}$	C5V66	C3	V5	60/90	
145C	C5V73	E3	V8	60/90	Step MQC at t2 following each subtraction until the Through-Zero signal is developed, then produce the OR CYCLE.
$\overline{145C}$	C5B71	E2	V7	60/90	
147A	B6T83	G3	V12	60/90	Sample (MQC-FT). If digit is < 3, reset the ≥ 3FF, this transfers (rL) to HSB and supplies one stepping pulse to MQC. If digit is ≥ 3, set the ≥3FF, this transfers (rF) to HSB and supplies three stepping pulses to MQC.
$\overline{147A}$	B6T87	G7	V14	60/90	
147B	B6T81	G2	V11	60/90	If digit in MQC-FT=0, set IER and IER-OR FF's at following t2.
$\overline{147B}$	B6T85	G6	V13	60/90	
149	B12T73	E3	V8	60/90	Inhibit generating a second IER CYCLE in the case that a decimal zero is set up in the MQC.
$\overline{149}$	B12T71	C7	V7	60/90	
151C	~~C3B60~~ C3V60	A6	V3	60/90	Disconnect rA input to comparator and connect rL.*
$\overline{151C}$	C3V33	A8	V4	60/90	

If $rL \leq rA$, Improper Dívison occurs at t2 of the eleventh minor cycle of PC-3.

* Sign comparison is performed on (rA) and (rL).

Function Table	Chassis	TT	Tube	S/NS	Definition
152A	C3V68	C5	V6	60/90	Disconnect rX input to comparator and connect HSB.*
$\overline{152A}$	C3V66	C3	V5	60/90	
152B	C3V42	E3	V8	60/90	Connect HSB to comparator.
$\overline{152B}$	C3V39	C8	V7	60/90	
153A	B8T75	E6	V9	60/90	Connect HSB to rX via sign reversal gates.#
$\overline{153A}$	B8T44	E7	V10	60/90	
153B	B8T81	G2	V11	60/90	Operate sign reversal gates in rX.
$\overline{153B}$	B8T48	G4	V12	60/90	
156A	C3V87	--	V14	60/90	Set up comparator to perform equality comparison.##
$\overline{156A}$	C3V85	--	V13	60/90	
156B	C3V48	--	V12	60/90	
$\overline{156B}$	C3V79	--	V11	60/90	
156C	C3V77	E7	V10	60/90	
$\overline{156C}$	C3V75	E5	V9	60/90	
159	B6T46	E5	V9	60/90	Retain results of comparison in comparator.
$\overline{159}$	B6T48	E6	V10	60/90	

* Sign comparison is performed on (rA) and (rL).

\# The sign reversal gates complement the LSB and Check Pulse of the sign digit during transfer to rX.

\## If rA = rL develop CT signal.

Function Table	Chassis	TT	Tube	S/NS	Definition
160A	C4V70	C7	V7	60/90	Operate adder for eleven-place addition.**
$\overline{160A}$	C4V71	E3	V8	60/90	
160B	C4V75	E5	V9	60/90	
$\overline{160B}$	C4V77	E8	V10	60/90	
160C	C4V79	G2	V11	60/90	
$\overline{160C}$	C4V81	G3	V12	60/90	
160D	C4V85	G6	V13	60/90	
$\overline{160D}$	C4V87	G7	V14	60/90	
161A	B12T44	E8	V10	60/90	Transfer sign from comparator to rA and rX.
$\overline{161A}$	B12T75	E5	V9	60/90	
161+	B12T81	G3	V12, 10	90/60	Inhibit the insertion of a decimal zero into rA.
$\overline{161+}$	B12T79	G2	V11, 9	90/60	
170	B10T75	E5	V9	60/90	Operate rA clear gate, except for sign position.
$\overline{170}$	B10T77	E7	V10	60/90	
171	B10T60	A17	V3	60/90	Insert decimal zero in LSD position of rA.
$\overline{171}$	B10T62	C11	V4	60/90	
172A	B9T31	A6	V3	60/90	Set up comparator to perform algebraic comparison.*
$\overline{172A}$	B9T29	A5	V2	60/90	
172B	B9T66	C3	V5	60/90	
$\overline{172B}$	B9T64	C1	V4	60/90	

** If decimal carry occurs from eleventh digit position, set Overflow FF. If Second Instruction Digit is a minus sign, overflow sets Stop FF.

* If rA > rL, develop CT signal.

Function Table	Chassis	TT	Tube	S/NS	Definition
185A	C1V77	E5	V9	60/90	Connect HSB to rL. Operate rL clear gate.
$\overline{185A}$	C1V83	G3	V12	60/90	
187	B9T75	E5	V9	60/90	Connect rL to HSB.
$\overline{187}$	B9T40	E3	V8	60/90	
188A	C5V77	E7	V10	60/90	With < 3 signal. Transfer (rL) to HSB.
$\overline{188A}$	C5V75	E5	V9	60/90	
188B	C5V83	G4	V12	60/90	Replace sign digit with a decimal zero. Set TO and STOP FF's after each Time-on minor cycle if IOS is in "One Addition".
$\overline{188B}$	C5V81	G1	V11	60/90	
188C	C5V87	G7	V14	60/90	With ≥ 3 signal. Connect rF to HSB. Step PC upon completion of each IER-OR CYCLE.
$\overline{188C}$	C5V85	G6	V13	60/90	
190	B3T78	E2	V9	60/90	Connect HSB to rF, and operate rF clear gate.
$\overline{190}$	B3T50	E7	V10	60/90	
192	B5T41	E2	V8	60/90	Connect rF to HSB.
$\overline{192}$	B5T74	E5	V9	60/90	
193	B3T29	(A3)A4	V1	60/90	Operate extract circuit in rF.*
$\overline{193}$	B3T28	(E5)C5	V6	60/90	
200	B11T66	C3	V5	60/90	Connect CR and CU (000000 00) to HSB.**
$\overline{200}$	B11T68	C6	V6	60/90	

* Transfer is controlled by (rF). If the LSB of the corresponding digit in rF is a binary zero, the digit from rM is read onto the HSB. If the LSB is a binary one, the digit from rM is replaced with a decimal zero.

** The four LSD's of (CR) are merged with eight decimal zeros from CU to make a complete word which is transferred to HSB.

Function Table	Chassis	TT	Tube	S/NS	Definition
201	B2T26	A2	V1	60/90	Operate HSB CR gate, operate CR clear gate.
203	C2V46	G1	V11	60/90	Connect CR1 to CR2. (LH Instruction sets up at t7 of Gamma T0)
203K	C2V28	A3	V1	60/90	To FTOC.
204	C2V83	G4	V12	60/90	Connect CR1 to SR Distributor Line.
206	B2T64	C1	V4	60/90	Supply EP.
$\overline{206}$	B2T65	C2	V5	60/90	
208A	C1V53	G7	V14	60/90	Connect HSB to CC.
208B	C1V51	G5	V13	60/90	Operate CC clear gate.
209A	B11T85	G6	V13	60/90	If Conditional Transfer FF is set, connect HSB to CC.
209B	B11T87	G8	V14	60/90	If CT FF is set, operate CC clear gate.
210	C2V44	E8	V10	60/90	Connect CC to HSB.
$\overline{210}$	C2V75	E5	V9	60/90	
212A	C2V62	A8	V4	60/90	Connect CC to adder min input.
$\overline{212A}$	C2V60	A5	V3	60/90	
212B	C2V71	E3	V8	60/90	Clear CC.
212C	C2V70	C7	V7	60/90	Transfer sum from unbarred adder to CC.
212D	C2V37	C5	V6	60/90	Connect CU (000000 000001) to adder sub input.
$\overline{212D}$	C2V66	C3	V5	60/90	
213CK	B8T87	G17	V14,13	-20/+5	Operate shift selector checker.
213	B10T70	C7	V7	60/90	Step PC once each minor cycle.*
$\overline{213}$	B10T73	E3	V8	60/90	

* If PC is advanced in excess of thirteen, an Overshift signal is developed which stops machine operation by setting FT Intermediate Checker FF and T0.

Function Table	Chassis	TT	Tube	S/NS	Definition
214	B2T51	G4	V12	60/90	Step PC, set TO.
$\overline{214}$	B2T52	G5	V13	60/90	
215	B7T68	C6	V7	60/90	Supply EP.
$\overline{215}$	B7T37	C5	V6	60/90	
217	B7T87	G7	V14	60/90	Set Stop FF if Comma Breakpoint switch is depressed.
$\overline{217}$	B7T85	G6	V13	60/90	
218	~~B8T79~~ B9T79	G1	V11	60/90	Set Stop FF.
$\overline{218}$	B9T44	E7	V10	60/90	
226	B10T64	C3	V5	60/90	Set Repeat FF.
$\overline{226}$	B10T37	C5 E5	V6	60/90	
228	B12T87	G7	V14	60/90	Reset Repeat FF at end of IER OR CYCLE.
$\overline{228}$	B12T85	G6	V13	60/90	
236	B9T85	G5	V13	60/90	Set Stop FF with CT Selector. Switch signals during Q or T instructions.
$\overline{236}$	B9T48	G3	V12	60/90	
244	B7T48	G3	V12	60/90	Set TO at end of IER OR CYCLE.
$\overline{244}$	B7T79	G1	V11	60/90	
245	B5T77	E16 E7	V10	60/90	Transfer 4 LSD's of (CC) and 000000 UO from CU to HSB.
$\overline{245}$	B5T79	G11 G1	V11	60/90	
246	C4V56	A2	V1	60/90	If rA or rX comp error occurs, set TO at following t1.
$\overline{246}$	C4V58	A4	V2	60/90	
248	B7T66	C3	V5	60/90	Connect CR to HSB.
$\overline{248}$	B7T62	A8	V4	60/90	
401	B2T49	E8	V10	60/90	Connect CU (000000 000000) to HSB.
$\overline{401}$	B2T50	G2	V11	60/90	

Function Table	Chassis	TT	Tube	S/NS	Definition
428	B11T58	A1	V1	60/90	Operate HSB-AOC.
$\overline{428}$	B11T57	A3	V2	60/90	
429	B11T62	A7	V3	60/90	Operate HSB-OEC.
$\overline{429}$	B11T64	C1	V4	60/90	
435A	B3T48	G4	V12	60/90	Operate adder OE and sum comparison checkers.
435B	B3T46	G2	V11	60/90	
604A	B4T42	E4	V9	60/90	Gate LE of FT604 to ending pulse delay.
604B	B4T54	A1	V1	60/90	
606	B4T31	A6	V3	60/90	Gate "0 Select" signal to determine if computer will pass interlock to start transfer operation.*
607	B4T50	G6	V13	60/90	Gate IRG to pick Interlock relay in Uniservo (n).
608	B4T64	C1	V4	60/90	Inhibit step PC, supply EP if Uniservo is rewound.
609	B4T79	G1	V11	60/90	If Direction Memory agrees with instruction, gate EP to control circuits.
609G	B4T46	No tube, test Point			To FTIC.
614	B4T77	E7	V10	60/90	Gate EP to set Read Forward and Start Read FF's after appropriate delay.
615	B4T48	G4	V12	60/90	Gate EP to set Write Forward and Start Write FF's after appropriate delay.**

* Computer will pass interlock if:
1. Read Interlock is reset.
2. Reversal Memory is reset.
3. IO INT-FF is reset.
4. First Block Memory is reset.
5. No rewind has been initiated within 3 ms.

** Length of time before Write Forward FF is set is determined by condition of Reversal Memory.

Function Table	Chassis	TT	Tube	S/NS	Definition
616	B4T73	E2	V8	60/90	Generate signal to pass Supervisory Control interlock provided that no read, Supervisory Control type-out, or Supervisory Control type-in is in progress.
617	B4T28	A4	V2	60/90	Gate IRP to set Supervisory Control Output FF, set Write Interlock.
619	B4T53	G7	V16 V14	60/90	Generate BP signal and supply pulse to initiate Rewind Start circuits.
621	B4T66	C5	V6	+5/-20	Gate IRP as Sequence I Preset.
629G	B4T38	C14	V5	30/90	Generate nS (servo select) signal from Second Instruction digit.
641+	B5V62	A18	V4, 1	+5/-20	Inhibit set of M_1 cores, strobe rI sense amplifiers, and transfer $M_2 \rightarrow M_1$ and $M_2 \rightarrow$ rI. Step rI address counters once for each word transferred until "59" signal occurs, at which time set MTO, step PC, and set TO.
641+	B5V71	E12	V8, 5	+5/-20	
641	B5V31	A16	V3, 4, 1	-20/+5	Permits the rI Preset error to be recognized during PC-2 only in the 3n or 4n instruction.
645+	B5V44	E16	V10, 9	+5/-20	Operate Input Distributor for type-in.
669	B7T58	A13	V2, 3	+5/-20	Gate IRP to generate Sequence 0 Preset.
681+	B4V41	E12	V8, 5	+5/-20	Transfer $M_3 \rightarrow$ r0. Step r0 address counters once for each word transferred until "59" signal occurs at which time set MTO, step PC, and set TO.
681+	B4V79	G11	V12, 9	+5/-20	
681	B4V38	E18	V11 12, 9	-20/+5	Permits the r0 No Address error to be recognized during PC-2 only of the 5n or 7n instruction.

Function Table	Chassis	TT	Tube	S/NS	Definition
685+	B5V81	G12	V12,11	+5/-20	Read M_3, transfer $M_3 \longrightarrow M_4$, type out digit on SC printer.
714A	B6T60	C1	V4	60/90	Operate adder for 12-place addition.
714A	B6T31	A6	V3	60/90	
714B	B6T35	C6	V6	60/90	
714B	B6T33	C4	V5	60/90	
714C	B6T77	E3	V8	60/90	
714C	B6T44	E2	V7	60/90	
737	C2V87	G8	V14	60/90	Enables a t1 pulse to reset the Overflow flip-flop.
737	C2V85	G6	V13	60/90	
816+	B7V30	A15	V3,1	+5/-20	When the rZW tens and units counters read zero, gate a t59 to set MTO.*#
816+	B7V67	C15	V6,4	+5/-20	
817+	B7V46	G12	V11,9	+5/-20	Preset rZW units counter to the elevens complement of the 2nd Instruction Digit. When counter reads zero, gate t59 to set MTO.
817-	B7V50	G17	V13,14,12	+5/-20	
817+	B7V52	G18	V14,12,8	+5/-20	
818+	B6V62	A17	V4,3	+5/-20	Enable the set of the rZW Read FF. When MTO is set, supply EP at following t1.
818+	B6V64	C12	V5,6	+5/-20	
819+	B3V76	E3	V9,8	+5/-20	Strobe rZW sense amplifiers.
820+	B2V27	A12	V1,2	+5/-20	Enable set of rM, rZW Read/Write FF's, set M_1 cores.
821+	B2V37	C15	V6,5	+5/-20	Generate Strobe rM signal.
823+	B3V55	C17	V2,1	+5/-20	Develop Staticize Pulse, Read M_1 cores, $M_1 \longrightarrow$ PS, M_1 to staticizer.
823	B3V83	G16	V14	60/90	

* If 2nd Instruction Digit is a 7, 8, 9, or 0, treat instruction as a Skip if Compatibility switch is set to Univac II.

\# If Compatibility switch is set to Univac I, the rZW tens counter is preset to zero.

Function Table	Chassis	TT	Tube	S/NS	Definition
824B	B2V31	A16 A7	V3 V4	+5/-20	Develop Serialize Pulse, Read M_1 Cores, $M_1 \rightarrow$ PS, $M_1 \rightarrow$ Serializer.
824A	B2V79	E16 E6	V11	60/90	Operate rM $\rightarrow$ HSB "extract" circuits.
$\overline{824A}$	B2V51	G8	V14	60/90	
825-	B4V55	A11	V1, 2	-25/gnd	Set MTO. X
$\overline{825-}$	B4V59	C11	V4, 3	-25/gnd	X
826+	B3V37	C15	V7, 6	+5/-20	Set rM and rZW Read/Write FF's, Set M_1 cores.
827+	B2V74	E18	V10, 9	+5/-20	Set BCM to RM.
$\overline{827+}$	B2V69	C18	V7, 8	+5/-20	
829+	B2V81	G2 G12	V12, 13	+5/-20	Transfer $M_1 \rightarrow M_3$.
831	B9T54	A1	V1	60/90	Complement the operation of the "extract" circuit.*
$\overline{831}$	B9T87	G7	V14	60/90	
832	B9T37	C6	V6	60/90	Disconnect CU (000000 000000) input to "extract" circuit, connect rA.
$\overline{832}$	B9T70	C7	V7	60/90	
833+	B6V79	G1	V11, 12	+5/-20	Step rM counters and rZW units counter once each minor cycle until rZW units counter reads zero.
$\overline{833+}$	B6V86	G7	V14, 13	+5/-20	
850	C1V47	G1	V11	60/90	Connect CC to SR via CR2.#
860+	B7V71	E12	V8, 7	+5/-20	Operate rM address exceeded and preset checkers.
860	B7V26	E11	V7	+30/+90	
861A	B7T47	~~A11~~ C17	V10, 1	-20/+5	Inhibit rM line drivers.
$\overline{861A}$	B7T41	~~E12~~ E11	V8, 1	-20/+5	
861B	B7T72	A11 E14	V9 V1	+30/+90	
Dummy 1	B8V26	A2 G12	~~V1~~ V12	60/90	Enforce order of "eveness" in FTOC.

RH Instruction set up at t7 of Delta TO.